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Use with the Following Devices

M88, M68, M64, Si5332, Si5334, Si5335, Si5338, Si5340, Si5341, Si5342, Si5342H, Si5344, Si5344H, Si5345, Si5346, Si5347, Si5348, Si5350, Si5351, Si5355, Si5356, Si5357, Si5371, Si5372, Si5380, Si5381, Si5382, Si5383, Si5384, Si5386, Si5388, Si5389, Si5391, Si5392, Si5394, Si5395, Si5396, Si5397, Si51210, Si51211, Si51214, Si51218, Si53352, Si53354, Si53358

Use with the Following EVBs

M88/M68/M64	M-EVK
Si5332	Si5332-12EX-EVB, Si5332-8EX-EVB, Si5332-6EX-EVB, Si5332-12IX-EVB, Si5332-8IX-EVB, Si5332-6IX-EVB, Si5332-8A-EVB (Si5332-AM2-QFN40-EVB), Si5332-6A-EVB (Si5332-AM1-QFN32-EVB)
Si5338	Si5338-EVB
Si534x/7x/8x/9x	Si5340-D-EVB, Si5340-EVB, Si5341-D-EVB, Si5341-EVB, Si5342-D-EVB, Si5342-EVB, Si5344-D-EVB, Si5344-EVB, Si5344H-EVB, Si5345-D-EVB, Si5345-EVB, Si5346-D-EVB, Si5346-EVB, Si5347-D-EVB, Si5347-EVB,Si5348-D-EVB, Si5348-E-EVB, Si5348-EVB, Si5372A-A-EVB, Si5372J-A-EVBs, Si5380A-D-EVB, Si5380-D-EVB, Si5381A-E-EVB, Si5381-EVB, Si5382A-E-EVB, Si5382-EVB, Si5383-D-EVB, Si5386A-E-EVB, Si5389-EVB, Si5391A-A-EVB, Si5391P-A-EVB, Si5392E-A-EVB, Si5394A-A-EVB, Si5394E-A-EVB, Si5394P-A-EVB, Si5395A-A-EVB, Si5395E-A-EVB, Si5395P-A-EVB, Si5397A-A-EVB
Si535x	Si535X-B20QFN-EVB, Si5356-EVB, Si5357-EVB
Si51211x	Si51211-EVB, Si51218-EVB

PC System Requirements

Operating System:

> ClockBuilder Pro (CBPro) requires Windows Vista Service Pack 2, Windows 7 Service Pack 1, Windows 8, or Windows 10. Either 32- and 64-bit versions are supported.
>
> CBPro uses Microsoft.NET Framework version 4.5. The installer will check to see if it is installed and, if not, prompt to automatically download and install it. Newer Windows operating systems will already have .NET 4.5 installed.
>
> If you need to install CBPro on a PC that does not have an Internet connection and does not have .NET 4.5, you can download Microsoft's stand-alone installer from http://download.microsoft.com/download/b/a/4/ba4a7e71-2906-4b2d-a0e1-80cf16844f5f/dotnetfx45_full_x86_x64.exe. Install .NET 4.5 before running the CBPro installer.

1024 x 768 screen resolution or greater

USB 2.0 or higher if you want to connect to a supported EVB

Export Regulations

ClockBuilder Pro (CBPro) is not authorized to create Orderable Part Numbers (OPNs) for products that are subject to export control regulations under ITAR. Do not use this software if you intend to create OPNs and do not have a license from the U.S. Department of State's Directorate of Defense Trade Controls (DDTC) to export the configuration files outside of the United States. Alternatives to OPNs are in-system volatile programming and customer managed non-volatile memory burn. Please review ClockBuilder Pro Tools & Support for In-System Programming documented bundled with CBPro for additional information and contact your local Silicon Labs sales office or distributor for assistance.

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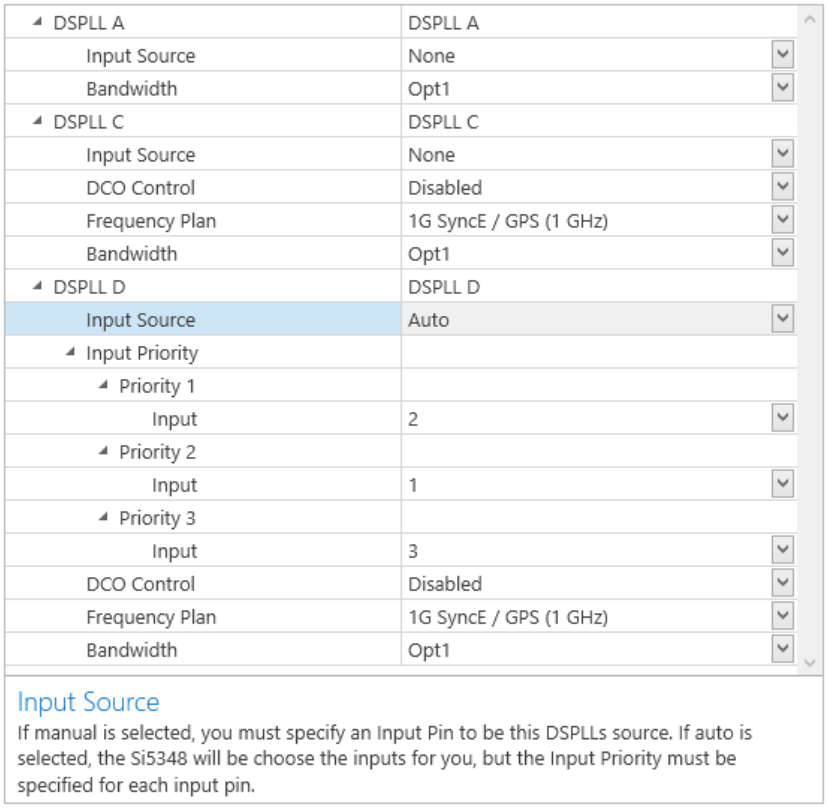
Version 3.0 [2020-11-15]

Added Support for Configuring M88/6x AccuTime Modules

- Available through new function in the CBPro part selector:

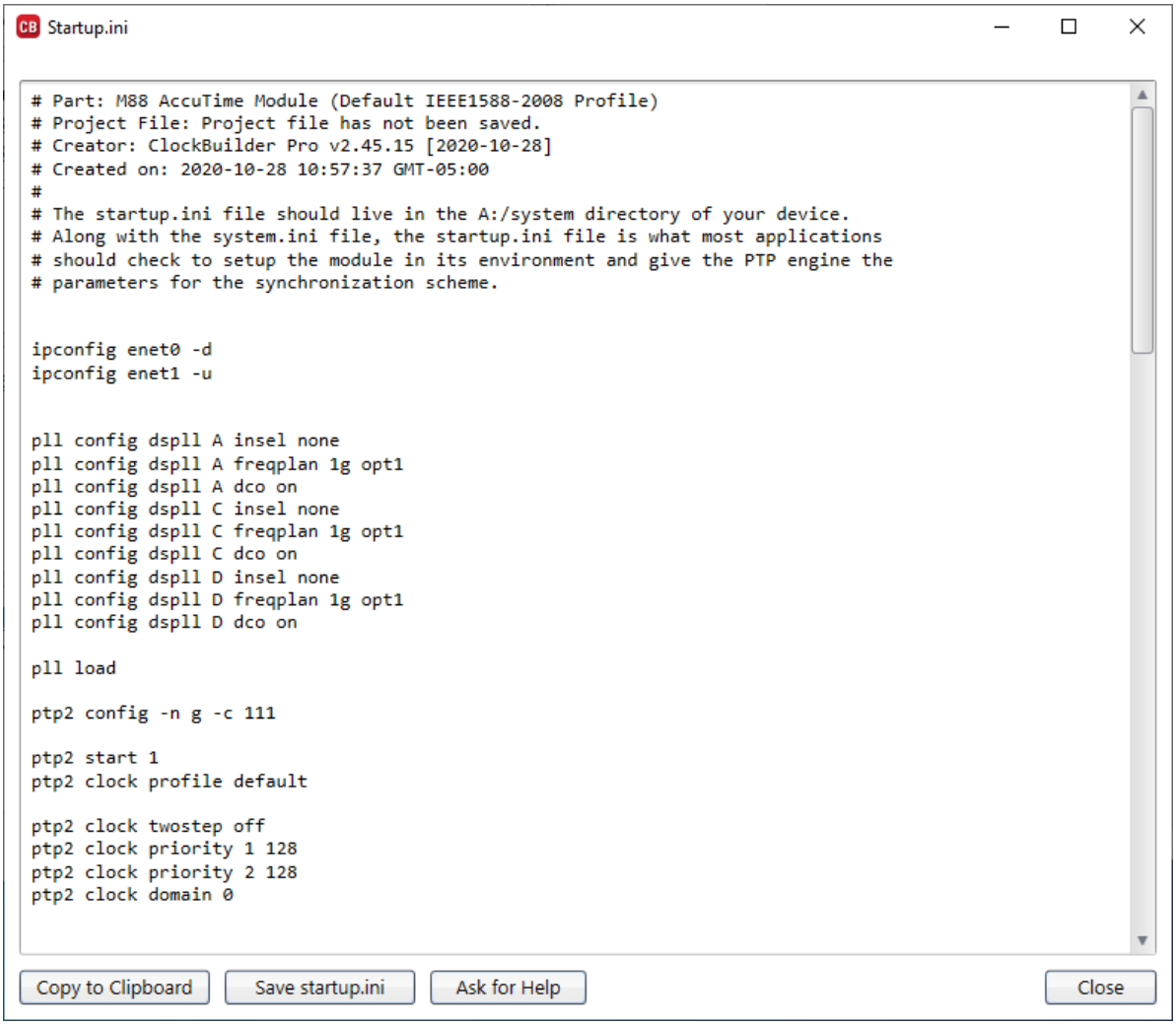


- M88, M68, and M64 part wizards step you through configuring the module:



- As with other CBPro supported devices, design rule checks are continuously run and verify functioning configuration

- When complete, use the Export tool to save a *startup.ini* file for your configuration:



Si5349/81/82/86

- Updated conditions under which input-to-output delay DRC warning is triggered: Fpfd < 1MHz without ZDM will trigger (TMGSW-1523)

Si5332

- Fixed: Multiprofile with GPIO_DIN_ENA_[L|H] setting varying between profiles will cause mcu to only load profile 0 (TMGSW-1426)
- Fixed: Output skew control was displaying 'Input Needed' when unused
- Fixed: Input clocks page was allowing user to continue with wizard even if no input was defined (TMGSW-1288)
- Fixed: NVM burn tool was failing when multiple Si5332/57 devices were in the same I2C Bus (TMGSW-1117)
- Added extra GPIO information to Datasheet Addendum (TMGSW-1466)

Si5351/50

- Fixed: 10-MSOP package was displaying crosstalk warning about frequencies not available in that package (TMGSW-1399)

Misc

- Fixed high DPI rendering issues (TMGSW-1113)

Added and updated support for pre-release devices

Version 2.45 [2020-07-16]

Misc

- Do not calculate estimated power if there is outstanding DRC error

Si534x/7x/8x/9x

- Si5392/4/5P/E: fixed: could not have both 125 & 200 MHz in the same project (TMGSW-1435)
- Fixed: defining an output as custom differential could cause DRC error that could only be cleared by making a change elsewhere; also, do not flag custom differential issues first time through the wizard (TMGSW-1116)

Si5334/35/38/55/56

- Removed option to “disable” output drivers from parts that do not have I2C to prevent users from accidentally order OPNs where outputs were stuck as disabled.
- Added DRC warning to alert the user that the OEB pin will not have effect on outputs set as “disabled”

Si51210/11/14/18

- Fixed: Output enable active state was confusing in GUI, removed “inversion mode” for “active state” (TMGSW-973)
- Fixed: GPI design report had active state backwards (TMGSW 1404, TMGSW-1386)

Added ITAR Export Control Notices (TMGSW-1417)

- CBPro has been updated to communicate that it should not be used to create Orderable Part Numbers (OPNs) for use with products that are subject to export control regulations under ITAR
- Information has been added to the release notes (README), installation guide (bundled in ZIP downloaded from silabs.com), and end-user license
- A new page has been added to the installer and OPN wizard that requires the user to acknowledge this restriction

Updates for pre-release devices

Version 2.44 [2020-06-11]

Miscellaneous

- Allow "no clock" configurations to be written to EVB and field programmer from CBPro wizard, allowing customer to mimic a similar OPN, which is fully supported

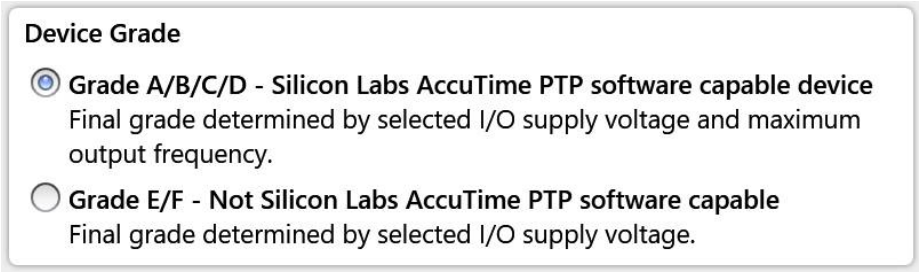
Si534x/7x/8x/9x

- Fixed: DUT dump was crashing when used with the field programmer (TMGSW-1371)
- Si5342H/44H/71/72: in register export scripts, for non-DCO configurations removed write to 0x0540 register in the “body” of the script in favor of postamble write. This reduces FCAL variability in more frequency plans when DCO mode is off. (TMGSW-1395)

- Si5348/83/84 RevD: if DSPLLD is set to manual input select mode and IN3 or IN4 are inputs to the PLL, force IN_LOS_MSK_PLLD and IN_OOF_MSK_PLLD bits 0:1 to 1 (i.e. lower two bits set to 3). This is to work around the following issue: If DSPLL D is set for "manual input select" and selects IN3, it goes LOL when IN0 is disabled (it doesn't matter whether this input is selected by other PLLs or not). The same issue occurs when DSPLL D is in manual input select mode and selects IN4 and IN1 is disabled. Rev E devices do not have this issue. (TMGSW-1396)
- For parts that support the FOTF CLI, added a button to the bottom of the output page that, when clicked, provides an overview of the tool and has links to the bundled documentation (TMGSW-1291)



- Si5388/9:
  - Allow Non-Standard CMOS and Pulsed CMOS (TMGSW-1380)
  - Support grade E/F via update to Mode page, now Grade & Mode (TMGSW-1316)



  - Updated mode diagram (TMGSW-1316)
  - Support CBProDeviceRead --all mode (CLI to dump all device register settings to console or file)
- Si5383/4/8/9: support DUT dump tool

Si5332/57

- Fixed: Tooltip for spread spectrum was calling SSON pin function instead of SSEN (TMGSW-1123)
- Fixed: Output skew wizard page description was listing step size in nanoseconds instead of picoseconds (TMGSW-1306)
- Fixed: Frequency plan was allowing output frequencies greater than 250 MHz on fractional dividers (TMGSW-1401)
- Wizard pages and datasheet addendum now show the device grade(s) supported for the current configuration (TMGSW-1027)
- Added better description for Pin MUX functionality and limitations (TMGSW-991)

Si5334/38

- Fixed: ac-coupled was misspelled (TMGSW-1295)
- Fixed: Incorrect part name in input and output wizard page description (TMGSW-1296)

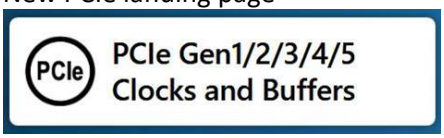
Si5350

- Modified the use of FIXREGs to enable the use of center spread for 10-MSOP devices

CBPro Home Screen and Part Selector Update (TMGSW-1378, TMGSW-1402)

- New documents added to welcome page
- Part meta-data updates

- New PCIe landing page



Updates for pre-release devices

Version 2.43 [2020-03-31]

Si5348/83/84/88/89

- Fixed: if DSPLLB (REF) LOL auto set thresholds was unchecked and the threshold values were changed from their defaults and the project saved, when the project was reloaded the threshold values would return back to their default values (TMGSW-1330)

Si5350/51

- Support 16-QFN packages
- Added support for users to specify synchronous and asynchronous output clocks for grade C parts
- Added support for user to set input pin as power down (PDN)
- Added custom CEVB DUT write window for emulating pin functionality as well as different packages. The user can now emulate frequency select, spread spectrum, and 10-MSOP/16-QFN parts on the Si5350/51-20QFN-EVB

Version 2.42 [2020-03-17]

Si5381/2/6

- Support lower loop bandwidth when Zero Delay Mode is enabled (TMGSW-1317)

Si5332

- Added Grade-L support for embedded crystal devices

Si5334/35/38/55/56

- Fixed: datasheet addendum was showing entry for Design ID which was not applicable to this part family (TMGSW-1269)
- Si5356: Fixed: Si5356-EVB was failing VCO calibration (TMGSW-1319)
- Si5334: Fixed: part selector wizard had incorrect input frequency range (TMGSW-1151)

Miscellaneous

- Update links on the Welcome screen

Version 2.41 [2020-02-05]

Si5334/38

- Fixed: CBPro was allowing setting IN1/2 and IN5/6 as single ended format (TMGSW-1040)
- Si5334: Added DRC error for configurations that use IN3 or IN4 and user choose incorrect input pin setup

Si5397

- Fixed: with Si5397A EVB attached, selecting ‘Open Default Plan’ changes XAXB frequency to 54MHz, causing lock issues; should be 48M (TMGSW-1294)

Version 2.40 [2020-01-21]

Miscellaneous

- The CBPro Overview presentation available from the welcome screen has been updated

Si534x/7x/8x/9x

- Fixed: DRC message "with the selected configuration, a Si539xE or Si539xP grade device would have lower jitter" was generated even when CMOS outputs are configured (TMGSW-1289)
- FOTF Changes (CBProFOTF1 CLI)
    - Fixed: on single PLL / clock generator devices could generate changes for other MultiSynth; for example, if N1 was being targeted in a set of plans, it was possible for N0 to be modified (TMGSW-1283)
    - The tool is faster for single PLL / clock generator case
    - Added support for Si5388/9
    - Updated user manual and in-system programming guide to reflect support for Si5371/72/88/89
- Si5388/9: added support for firmware v1.2 (TMGSW-1266)
    - This is the default for new projects
    - The EVB sample project uses this version as well
    - Existing projects can change to it on the Revisions page
    - Please contact your Silicon Labs representative for additional information

Si5334/35/38/55/56

- Fixed: the Si5338/56 field programmer was being detected by EVB GUI, causing it to crash (TMGSW-1243)
- Si5334/8: added option for "CMOS Single (Only B)" in output format dialog (TMGSW-1148)
- Added support for clock names in the input/output frequency entries (for example, "CLK1*2") (TMGSW-1114)
- Si5338/56: removed old copyright comment from “C header” export file

Version 2.39 [2019-12-11]

Si5350/51

- Fixed: Unused PLL was set to auto reset on LOL causing INTRB to trigger every 25 ms (TMGSW-1196)
- Fixed: CBPro wizard was allowing CLK6 and CLK7 to be set to 200 MHz causing frequency plan calculation to lock application (TMGSW-1186)
- Added feature to allow users to invert any output (TMGSW-1144)

Si5338

- Fixed: EVG GUI was crashing when the application could not talk through I2C with the DUT (TMGSW-1185)
- Fixed: Setting an output as CMOS complementary was keeping output as in-phase (TMGSW-1242)

Si5332/57

- Fixed: EVB GUI first regulator current was always high after a power cycle (TMGSW-1226)
- Fixed: EVB GUI was losing communication with the DUT after assigning an “I2C Address Pin” (TMGSW-724)
- Added support for users to disable internal crystal for embedded crystal grades E/F/G/H (TMGSW-982)
- Added I2C base address to Datasheet Addendum (TMGSW-1233)

Si534x/7x/8x/9x Miscellaneous

- Fixed: CBPro could crash if design report was open and DCO enable state was changed (TMGSW-1246)

- Fixed: CBProRegistersToSettings and CBProSi534x8xFirmwareExport CLIs did not return CBPro version when invoked with --version argument
- Si5349/81/82: Support fractional Px input dividers (TMGSW-974)
- Add DRC error if gapped clock less than 10MHz, to match datasheet (TMGSW-633)
- Si5392/4/5EP: removed pulsed CMOS input option; if an existing project has this selected, a DRC error will be generated (TMGSW-1050)
- FINC/FDEC pins on CEVB now de-asserted in CBPro launch (TMGSW-1245)
- Si5383/84: allow XTAL frequency down to 24.97M (25M with margin) to match datasheet (TMGSW-1238)
- On parts that allow XTAL reference below 48MHz, generate DRC warning if any frequency less than 48M is selected (TMGSW-1276)

  Incompatible XTAL frequency XXX MHz [1]

  [1] For optimal jitter and phase noise performance, Silicon Labs requires the use of 48 to 54 MHz XTALs compliant with the specifications noted in the Si534x/8x Family Reference Manuals. Using XTAL frequencies other than these may be possible, but jitter and phase noise performance may be degraded. Contact Silicon Labs to determine the impacts on your configuration.

  Previously 25M was special cased and a DRC warning was not generated. The change is to now generate the DRC warning even for 25MHz XTAL
- Don't generate "You cannot mix 1Hz/1pps and non-1Hz/1pps inputs on DSPLL D" DRC if current configuration is not even 1Hz capable
- Fixed: firmware export tool did not remember previous settings

Si5386

- Simplify DRC warnings if there is a fractional P divider
- Higher bandwidth can be achieved with fractional P dividers

Si5388/89

- Setting/register export now supported (TMGSW-1253)
  - If the device is already in network synchronizer mode, the register script can be used to reconfigure the device
  - In T-BC / T-TSC mode, full reconfiguration can only be performed by re-flashing the device configuration. Device setting/register values are provided for partial reconfiguration use cases and informational purposes only.
  - A header in the export files explains this
  - Multi-project export is not supported
- Design report now includes register/setting table (TMGSW-1253)

Version 2.38 [2019-10-31]

Miscellaneous

- CBPro now requires Microsoft.NET version 4.5 or higher
- Windows XP is no longer supported
- CBPro now uses less memory, especially on high DPI / 4K displays
- Fixed: link to "AN1077: Selecting the Right Clocks for Timing Synchronization Applications" on welcome screen was broken (TMGSW-1191)
- Fixed: if an EVB was connected and the “sample plan” was opened from the CBPro Welcome screen or you double clicked a supported project in Windows Explorer, you could be prompted multiple times to write the project to the EVB (or even hang) (TMGSW-607)
- Fixed: silabs.com password in Orderable Part Number (OPN) wizard was not being restored (TMGSW-1021)

Si5332/57

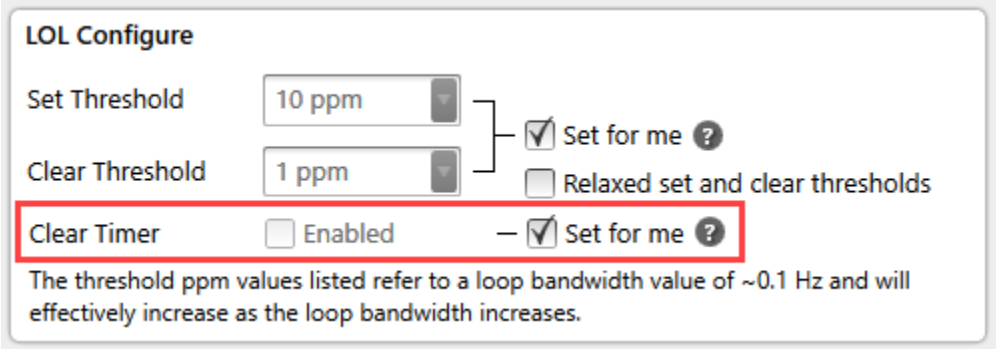
- Fixed: Frequency planner was failing to find solutions for plans that needed a higher VCO frequency in order to avoid running out of fractional MultiSynth dividers (TMGSW-895)
- Fixed: Automotive grade CEVB's first regulator reading was high by a few milliamps (TMGSW-1226)
- Fixed: Reset can only be assigned to specific universal hardware pins (TMGSW-1232)
- Fixed: CBPro was only showing Si53354B as a single input buffer instead of a two input buffer (TMGSW-1229)
- Added functionality for users to compare design estimates to Automotive grade CEVB measurements (TMGSW-1222)

Si5350

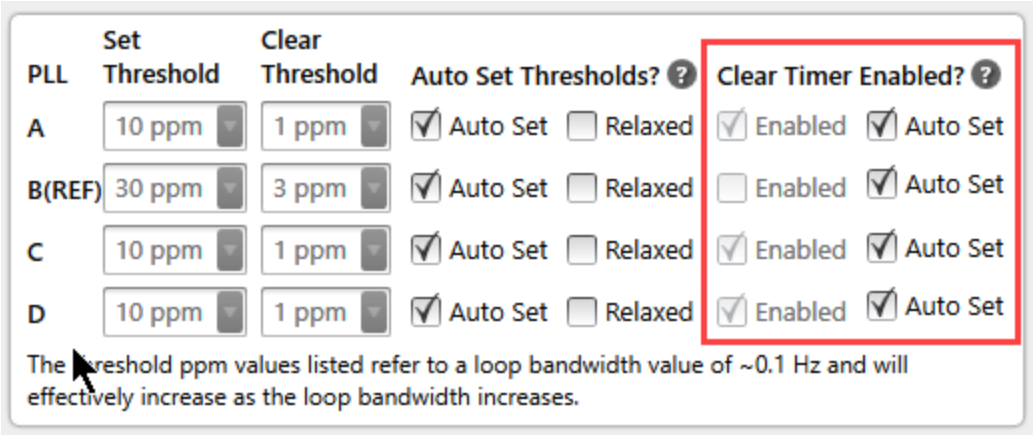
- Fixed: VCXO's APR range maximum was 120 ppm instead of 240 ppm (TMGSW-1150)

Si534x/7x/8x/9x

- Fixed: Si539xE/P: the Nx divider widget did not update when a change in frequency would cause a different divider to be used (TMGSW-1225)
- Fixed: CBProDeviceRead --all gives error "read of 326 bytes would span multiple register PAGE boundaries" (TMGSW-1198)
- Allow no clock design to be burned to NVM via field programmer (TMGSW-1195)
- Provide independent configuration for "Enable ramp at initialization" on DSPLL page independent of ramping mode. This applies to die B0+ devices. The default is on which maps to existing CBPro behavior (TMGSW-1107)
- Si5371/2: add documents to dashboard (datashort, EVB user's guide, and AN1206) (TMGSW-701)
- LOL clear timer changes (TMGAPPS-350, TMGSW-1018)
    - Provide editor for LOL clear timer enable and "set for me" mode
    - Affected devices:
        - Si5342/44/45/46/47/80/83 Rev D
        - Si5348/49 Rev D/E
        - Si5381/2/6 Rev E
        - Si5370/71/88/89/92/94/95/96/97 Rev A
    - If existing CBPro project opened, there will be no change to configuration or operation unless you actively change the configuration; details below
    - LOL page changes for single PLL device such as Si5345 Rev D and Si5395 Rev A:



    - LOL page changes for multi-PLL parts such as Si5348 Rev E:



- The LOL clear timer is recommended for loop bandwidth values less than 40 Hz. When the timer is enabled, the lock acquisition will be faster, but LOL assertion time will be longer. When ”set for me” / “auto set” is checked, CBPro will set the clear timer enable setting based on the effective loop bandwidth for the PLL.
- “Set for me” / “Auto set” is enabled by default for new projects
- For existing projects where the clear timer was never enabled, set for me is off and the timer is still disabled, to match previous behavior
- The device configuration is modified as follows:
  - Set FASTLOCK_EXTEND_MASTER_DIS (0x00E5[0]) to 0 always
  - Set FASTLOCK_EXTEND_EN (0x00E5[5]) / FASTLOCK_EXTEND_EN_PLLx (0x00E5[4..7]) to 1 when clear timer is enabled
  - Set LOL_TIMER_EN (0x00A[1]) / LOL_TIMER_EN_PLLx (0x00A[0..3]) to 1 when clear timer is enabled
- All sample projects that are bundled with CBPro have been updated to turn on LOL clear timer "set for me" mode

Version 2.37.0.1 [2019-09-26]

Si5332:

- Fixed: CBPro was not enabling OMUX5 causing outputs tied to VDDO5 to be disabled (TMGSW-1194). This bug was introduced in CBPro 2.37.

Version 2.37 [2019-09-22]

Added Support for Si53352/4/8 Output Clock Buffers

- Device can be simulated with a Si5332 AM Evaluation Boards (Si5332-AM2-QFN40-EVB and Si5332-AM1-QFN32-EVB)
- Custom factory programmed parts (Orderable Part Numbers) can be created

Si5332

- Support automotive grade packages AM1 and AM2
- Support Si5332-8A-EVB (Si5332-AM2-QFN40-EVB) automotive EVB
- Support Si5332-6A-EVB (Si5332-AM1-QFN32-EVB) automotive EVB

Si537x/8x/9x

- The Hitless Input Switching Assistant threshold for using ramped input switching – instead of hitless switching – was tightened from ± 10 ppm to ± 5 ppm. This more conservative approach minimizes output clock phase

transients by insuring that hitless switching, by default, will only be used for input clocks that can differ by a maximum of + 5 ppm - (-5 ppm) = 10 ppm total. (TMGSW-1180)

Miscellaneous

- CBPro now runs as a 64-bit process
- CBPro should consume less memory in most workflows
- CBPro about screen provides a way to get more details about system and install
- Fixed: in the multi-project export GUI, the 'Copy project file to output folder' and 'Create C code configuration scripts' checkbox effect on export were swapped

Updates for pre-release devices.

Version 2.36 [2019-09-04]

Si5338/56

- Added Field Programmer dongle support
- Added support for legacy Field Programmer
- Added export of NVM register file to be used with Legacy Field Programmer
- Added EVB GUI support
- Design report now shows lowest jitter output option is one selected
- Fixed: Mod rate for NVM spread spectrum was displaying 0 kHz (TMGSW-818)
- Fixed: Frequency plan overrides were not being used when solving for a solution (TMGSW-1100)
- Fixed: Configuring 4 outputs as buffers was displaying frequency plan error (TMGSW-993)
- Fixed: CBPro was allowing RESET pin to be configured to P5 and P6 contradicting the datasheet (TMGSW-1033)

Si5335/55

- Fixed: Datasheet addendum was not displaying output voltage (TMGS-981)

Si51210/14

- Added support for Rev B

Si534x/9x

- Fixed: the Si5345->Si5395 project converter had these issues:
  - If an input or output was used in OUT9 frequency, OUT9A would show an error after conversion
  - If OUT9 was used in another clocks expression, it was not converted to OUT9A and so would show an error after conversion
- Fixed: in select projects, enabling the hitless switching helper would cause the frequency planner to abort and generate a DRC error (TMGSW-1163)
- Fixed: Si5346/47/96/97: the frequency planner might not find a solution when input frequency was less than 100 kHz (TMGSW-1166)

Si5383/4/8/9 NVM Burn Tool Improvements (TMGSW-1158)

- Fixed: stop looking for ACK after final “execute program” bootloader command which could cause download tool to report error even though device was now back in program mode
- In each programming step, better inspection of bootloader response code and code-specific messages reported on and will stop programming
- Add option to accept a bootloader programming file

Updates for pre-release devices.

Version 2.35 [2019-06-18]

Si538x/9x:

- Add support for Si5392/4/5/6/7 Grade J/K/L/M integrated reference
- Add support for Si5392/4/5 Grade E integrated reference
- Si5388/89: support config/firmware flash image export for all customers

Si5332:

- Fixed: field programmer NVM burn was clearing out crystal trim settings for embedded crystal grades (TMGSW-1125)

Version 2.34.1 [2019-05-31]

CBPro Programmer:

- Fixed: dongle would not be detected if socket was not attached

Version 2.34 [2019-05-29]

Si5332

- Factory VCO calibration is now disabled for new Orderable Part Numbers (OPNs) in favor of device VCO self-calibration at power-up (TMGSW-1108)

Si534x/7x/8x/9x

- Fixed rare crash during DCO control update (TMGSW-1110)

Version 2.33 [2019-05-12]

Added Support for Si5371/2 Jitter-Attenuating, Single-PLL Coherent Optics Clock with Integrated Reference

Si5332

- Fixed: Frequency plan solver was calculating wrong P value when XA/XB had been previously configured and CLKIN1/CLKIN2 were being used with InSEL enabled (TMGSW-1074)
- Fixed: Pin configuration was keeping selections when setting to ‘none’ and incorrectly writing settings (TMGSW-1076)
- Fixed: Profiles pages and driver format page was showing 0Hz frequency when output is a buffer (TMGSW-1067)
- Fixed: wizard was allowing users to create pin controlled spread spectrum designs with unassigned SSEN pin (TMGSW-1106)
- Modified spread spectrum behavior to clear current configuration when there are no outputs assigned to its respective N divider (TMGSW-1084)
- GUI now allows the user to configure the default spread spectrum state when is being controlled by register

Si5350B

- Fixed: CBPro was overwriting VC pin when the general-purpose hardware input P0 was configured (TMGSW-1088)

Si534x/7x/8x/9x

- Fastlock, Hitless Switching (HSW) Assistant Improvements (TMGSW-670)

    - The HSW assistant will enable fastlock if actual loop bandwidth is <=20 Hz
    - New DRC if the HSW assistant disables fastlock and actual LBW is > 20Hz
    - New DRC if fastlock is disabled and actual LBW is <=20 Hz (not using HSW assistant, manually disabled fastlock)
- Si5383/4: fixed: CBPro error when P divider is fractional and DSPLLD is in 1pps mode (TMGSW-1097)
- Si5348 Rev E: resolve issue with creating an Orderable Part Number
- Si5349/81/82/86 RevE, Si5392/4/5/6/7 Rev A: updated input clock buffer mode descriptions to be more clear; added explicit “Non-Standard CMOS” option which ensures that IN_CMOS_USE1P8[x] is 0 for the selection (TMGSW-1078)

Updates for pre-release devices.

Version 2.32 [2019-04-10]

Miscellaneous

- Fixed: CLI documentation links on last slide of "CBPro Tools & Support for In-System Programming" were broken (TMGSW-1065)

Si5332

- Fixed: Assigning output as buffered was not adding correct power consumption to estimate (TMGSW-1056)
- Fixed: GUI was losing FSEL pin assignment in Output Configuration page after reopening project (TMGSW-984)
- Fixed: GUI was allowing user to select 1.8V for LVPECL (TMGSW-946)
- Fixed: OPN wizard was displaying external crystal grades in text description for encapsulated crystal (TMGSW-975)
- Fixed: Host Interface configuration was allowing the selection of invalid I2C address (TMGSW-1063)
- Fixed: Multi-profile configurations were not properly terminated in NVM causing OPNs to sometimes display erroneous outputs
- Updated Theta JA parameters in power estimation model for a more accurate estimate (TMGSW-1046)
- Added “debug dump” to EVB GUI which dump NVM, XREGs, and DPRAM
- Added GUI support to be able to select LVCMOS as CLKIN1/CLKIN2 format
- The default ambient temperature for Tj estimation was changed to 25C

Si534x/7x/8x/9x - Miscellaneous

- Fixed: Si5371/2: in the part selector, max Fout was listed as 2.75 MHz instead of 2.75 GHz (TMGSW-1061)

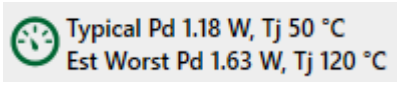
Si534x/7x/8x/9x - Power, Temperature Estimation Improvements

- Improved power (and therefore junction temperature) estimation model and GUI:
    - Improved accuracy in most cases
    - User entry of custom Theta-JA is now supported
    - The default Ta and JEDEC board selections have changed:
        - Ta: 25C
        - JEDEC: 0 m/s airflow for Si5380/6; 2 m/s for all others

  Note: Existing project files will get switched over to the new default
- For Si5349/80/81/82/86, worst-case Tj and power are estimated in addition to typical that uses the Ta entered by the user. Worst-case:
    - Ta = 85C
    - All supplies at Nominal+5% voltage
    - Takes into account increased leakage current possible at the extremes of normal process variation

It is expected that this combination of conditions will be very unlikely to occur, and is provided to give guidance for maximum current requirements.

- When worst-case is calculated, it will appear in the power widget in CBPro and power/design report:

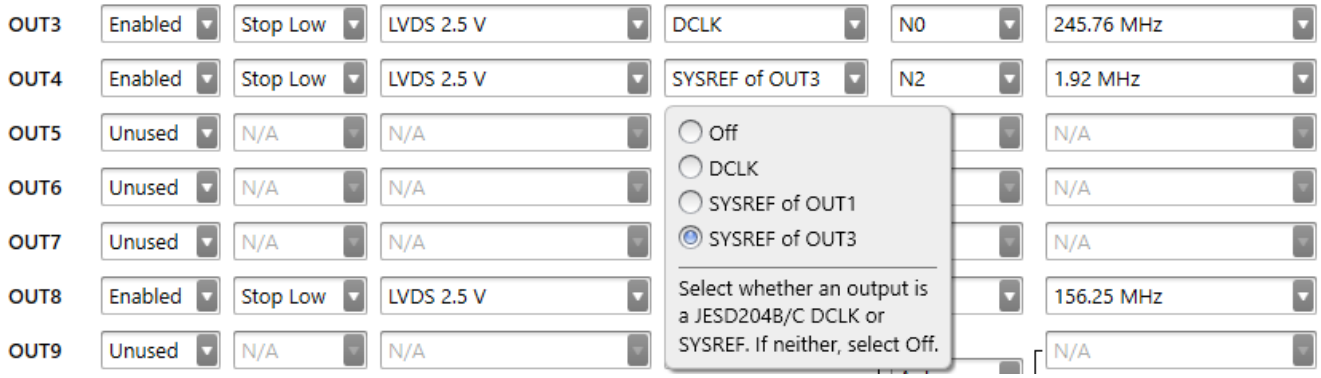


Condition	On Chip Power	Overall Power	Ta	Tj
Typical Ta, Voltage, Current	1.135 W	1.185 W	25 °C	50 °C
Worst-Case Ta, Voltage, Current	1.577 W	1.631 W	85 °C	120 °C

	Frequency	Format	Typical			Worst-Case		
			Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
VDD			1.8	236	424	1.9	417	788
VDDA			3.3	132	436	3.5	138	478
VDDO0A	153.6 MHz	LVDS	2.5	16	41	2.6	17	46
VDDO0	30.72 MHz	LVDS	2.5	16	39	2.6	17	44
VDDO1	491.52 MHz	LVDS	2.5	18	44	2.6	19	50
VDDO2	1.92 MHz	LVDS	2.5	16	39	2.6	17	44

Si5380/81/82/86 - Updated JESD204B/C Clock Identification

- JESD clocks are identified on the Outputs page:

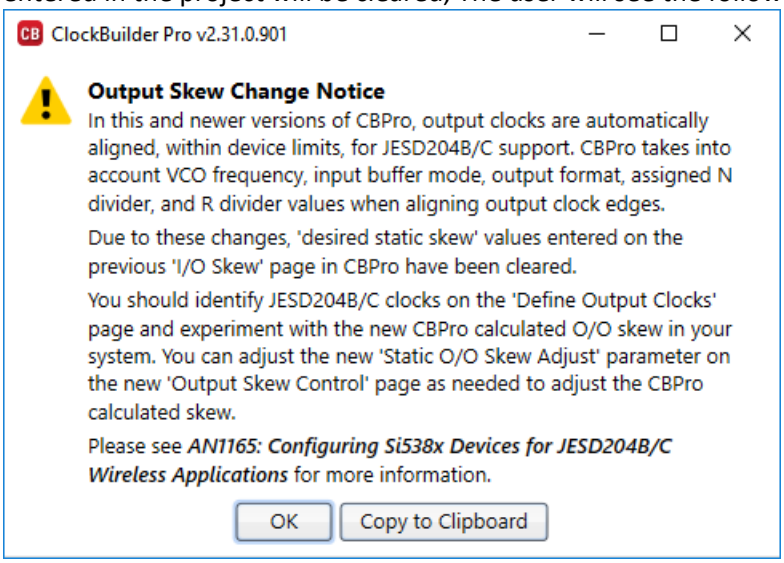


- DCLK integer relationship to VCO frequency is enforced
- SYSREF relationship to its DCLK is enforced
- JESD clocks must be manually assigned to an N divider (enforced by CBPro)

Si5381/82/86 Rev E - Reworked Static Skew Control

- CBPro will automatically calculate overall I/O delay for each output based on input buffer mode, output format, assigned N divider, and R divider values
- CBPro will then, within device limitations, align all JESD204B/C clocks to a common clock rising edge
- Customer may now specify an output-to-output skew adjust on top of the baseline alignment
- **Due to these changes, CBPro will write different register values for Nx_DELAY, Nx_IODELAY_STEP, and Nx_IODELAY_COUNT_compared to previous versions and overall I/O delay will be different for the same project file**

- When opening a project file created with an earlier version of CBPro, any existing 'desired static skew' value entered in the project will be cleared, The user will see the following notice:



- A detailed O/O skew report is in the design report
- See “AN1165: Configuring Si538x Devices for JESD204B/C Wireless Applications” for more information

Si5349/80/81/82/86 - Miscellaneous

- Si5380/81/82/86: EVB sample projects have been updated
- Si5349/80/81/82/86: Hitless switching is disabled by default on DSPLL B; if enabled, a new DRC warning is issued
- Si5349/81/82: the default input MUX configuration for new designs has been updated
- New DRC warning when DSPLL B shares an input clock with DSPLL A/C/D, DSPLL B has fastlock disabled, and DSPLL A/C/D has HSW/ fine HSW enabled (transient behavior on DSPLL B may have a stronger effect on the other DSPLLs under these conditions) (TMGSW-919)
- Si5381/82: new DRC warning if an output on DSPLL A/C/D requires an integer Nx divider (degraded jitter) (TMGSW-900)
- Si5386: fixed: various fractional P divider related settings/registers were not included in setting/register export files; this would cause the device not to lock if there was a fractional P divider and the corresponding input was selected (TMGSW-1059)

Updates for pre-release devices.

Version 2.31 [2019-03-25]

Si534x/8x/9x:

- Si5395: modified project conversion from Si5345 to Si5395: map OUT9 to OUT9A (TMGSW-1039)
- Si5380/86/91/95: the output diagram was updated to show R dividers (TMGSW-992)
- Si5342H/44H DCO changes (TMGSW-1045)
    - Removed the DCO mode selection: only direct register mode is supported (no FINC/FDEC)
    - The design report now always shows the direct register write equation
    - MXAXB_FSTEP_MSK and MXAXB_FSTEPW are excluded from the design report, exports, etc.

Si5391/2/4/5P: (TMGSW-1035)

- Input/output frequency ranges have been updated
- Input format: only “Standard” mode is supported on IN2/IN3 (no LVCMOS, no Pulsed CMOS, no single ended of any type)
- Output format: custom differential has been removed; HCSL is restricted to 25/50/100/125/200 MHz

- The fixed N divider assignments have been updated
- The EVB sample projects have been updated
- An output's P-Grade status/capability is reported via a new widget on the output page; the coupling check is still performed, but is only shown if there is a coupling issue not covered by one of the P-Grade rule checks for domain 1 (156.26/312.5/625 MHz) frequencies

Updates for pre-release devices.

Version 2.30.1 [2019-02-19]

Si534x/8x/9x: fixed: clicking a checkbox on the INTRb mask page had no effect

Version 2.30 [2019-02-19]

Si534x/8x/9x:

- Fixed: Si5340/41/42/44/45/81/82/86/91/92/94/95: the frequency planner could not always find a solution when an output had a high resolution fractional component; example, 322*419020819/418995225 MHz (TMGSW-988)
- Fixed: if DCO was enabled on a PLL and then it is changed to free run only mode, you would receive an error when trying to calculate the frequency plan
- Si5392P/94P: improved phase noise performance (TMGSW-827)
- Si5391/2/4/5P: disabled export for in-system programming; please contact Silicon Labs for assistance
- Si5380/81/82/86, Si5391/2/4/5P: increase preamble delay from 300 ms to 625 ms to account for worst case device calibration time
- Si5340/1 Rev B,D: I/O Skew support removed
- Si5346/47/96/97 All PLLs, Si5348/83/81/82/88 DSPLL A/C/D: when possible, select fractional P divider to keep Fpfd >= 100 kHz, resulting in less output jitter in some cases (TMGSW-1019)
- Si5380/81/82/86: changed the minimum loop bandwidth to 20 Hz on DSPLLB when XO selected (TMGSW-1017)

Si5335:

- Fixed: datasheet addendum did not show assigned output voltage (TMGSW-981)
- Fixed: CBPro and datasheet contradicted RESET function pin assignment (TMGSW-1033)

Updates for pre-release devices.

Version 2.29 [2018-11-4]

Si534x/7x/8x/9x:

- Fixed: the I2C address burn tool gave "Object reference not set to an instance of an object" error
- Update CBProFOTF1 CLI to support frequency-on-the-fly (FOTF) on multi-PLL devices when PLL is in "free run only" mode
- Using field programmer and socket, support burning NVM when target device and project file SPI mode do not match. I.e. target is configured for 4-wire and project is 3-wire (and vice versa). The support is automatic: there is nothing for user to do.
- Coupling (crosstalk) DRC footnote explains harmonic contribution to the coupling check

Si5332:

- Fixed: a device that had NVM burned using the field programmer with CBPro 2.27.2 through 2.28.4 would not operate normally when coming out of reset; any parts programmed with this version can be recovered by burning the desired configuration a second time with CBPro 2.28.5 or higher
- Fixed: writing Si5357 project file via field programmer over-wire was causing a part mismatch error

Si5334/38:

- Fixed: EVB DUT write was failing PLL calibration when input source was IN4 or IN5/6

Updates for pre-release devices.

Version 2.28.1 [2018-09-24]

Support Si5348 Rev E (Network Synchronizer for SyncE/ 1588 PTP Telecom Boundary (T-BC) and Slave (T-SC) Clocks)

Version 2.28 [2018-09-24]

Si5332:

- Fixed: MultiSynth dividers were keeping spread spectrum settings even though outputs were set to “Auto” divider
- Fixed: GPIOs were configured backwards for Multiprofile, for example, LSB was being set as MSB
- Fixed: Multi-profile NVM required size calculation was missing 2 bytes per frame
- Fixed: Setting output as buffer was displaying corresponding R divider as being unused
- Fixed: multi-profile GPIO configuration was adding extra bytes for unused pins when translated to NVM
- Fixed: output buffer was triggering DRC error when bank was previously set to divider
- Fixed: C code header export had 16-bit addressing instead of 8-bit
- Add one time Field Programmer support for multi-profile projects

Si5335/55:

- Fixed: FS pin assignments in the GUI were swapped for 3 profile configuration. P1 was FS0 and it should be FS1 and P2 was FS1 and should be FS0. This was not causing a functional issue but it was not in agreement with the datasheet. Pin frequency select behavior is now driven by number of profiles
- Fixed: DUT Write read back was failing because of REVID setting is read-only, when writing to EVB this setting is now ignored
- Fixed: DUT Write was hanging when trying to perform the VCO calibration step if no signal is provided, the DUT write now fails gracefully after 500ms
- Enabled the ability for users to specify loop bandwidth at a profile level, rather than being global

Si534x/7x/8x/9x:

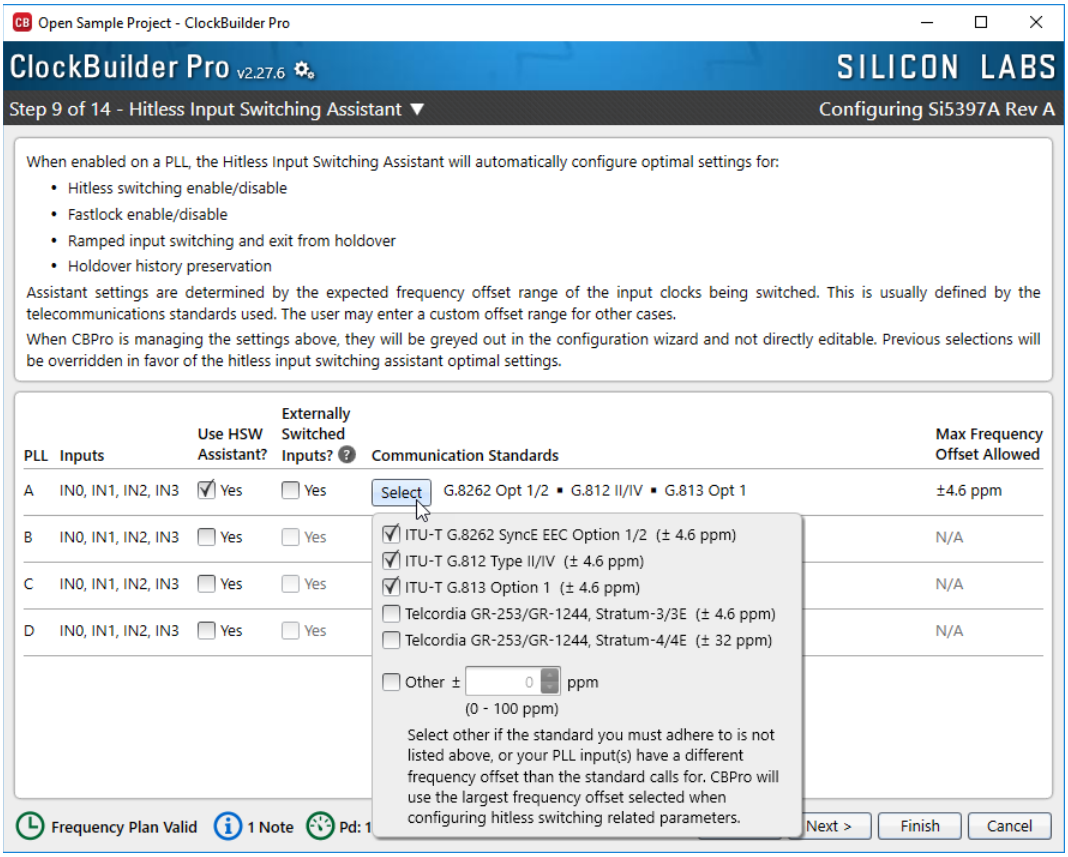
- Si5380: Fixed: DRC warning "When in Zero Delay Mode, because N0 is within the feedback loop, any phase/delay adjustments to the output clocks coming from N0 will have no effect" was shown even when ZDM was not enabled
- Support static I/O skew adjust on Si5381/2/6 Rev E
- Removed support for static I/O skew adjust feature on new Si5342/44/45 Rev B/D and Si5342H/44H Rev C/D projects. If any existing project has a non-zero static I/O delay value, the feature will continue to be available and further exits can be made to the project file. See PCN 180920394 Si5342-44-45-46-47 Rev D Datasheet and Crystal/TCXO/OCXO Ref. Manual Update.
- Improve Si5341/45 -> Si5391/95 Project Conversion:
    - Fixed: if OUT0 or OUT9 in the original 41/45 projects had manual N divider assignments and OUT0A or OUT9A were later enabled in the 91/95 project, there was a frequency planner error; future converted projects will not have this issue; if any previously imported project has this issue, you can fix the new project by temporarily changing the divider assignment to Auto and then back to the specific divider
    - OUT0A and OUT9A disabled state is now set to the existing OUT0 and OUT9 value
    - OUT0A and OUT9A output frequencies are set to OUT0 and OUT9 respectively (but still set to Unused)

- No longer distinguish between harmonic and significant crosstalk in output page [!] icon color and tooltip: always show solid yellow and use phrase "may have coupling" in the tooltip
- Frequency-on-the-Fly (FOTF):
    - Added support for FOTF on Si5348/83/84 with the following restrictions:
        - DSPLL B inputs, outputs, bandwidth, etc. cannot be adjusted
        - On Si5383/84/89, if a 1 Hz (1pps) input is present, DSPLL D cannot be adjusted
        - A 1 Hz output frequency cannot be set in a plan file; it can only be present in the base project (but can be switched to non-1 Hz in a plan)

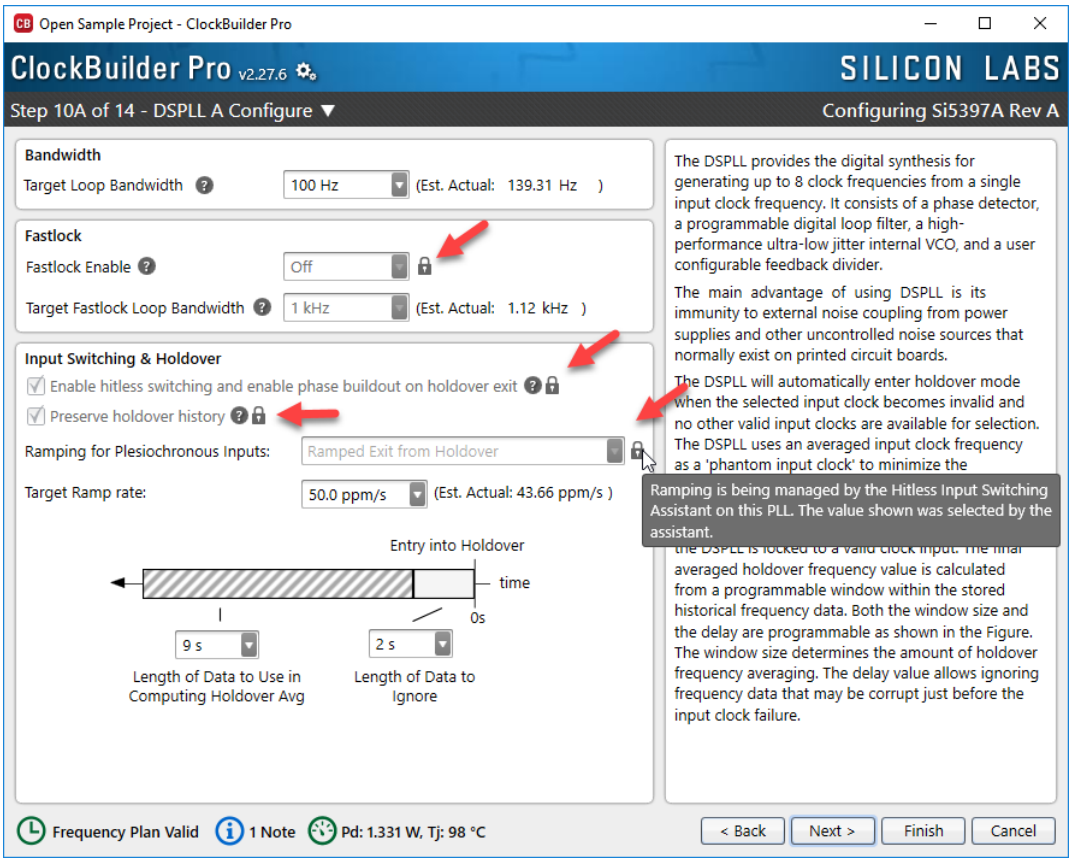
      All of the restrictions above are enforced by the tool
    - Further restrict multi-PLL such that FOTF is not supported on a PLL that has an input that is shared with another PLL
    - Update user manual and in-system programming overview to reflect this
- Move output disabled state and format to existing output frequency pages for all parts

New Si5381/2/6, Si5392/4/5/6/7, Si5348 Rev E Hitless Input Switching Assistant:

- A new page is available in the wizard, before the DSPLL page:



- When assistant is enabled on a PLL, the settings managed by it are auto set and locked:



- Bandwidth recommendations are made via DRC notes:

Ignore?	Category	Message	Note
☐	Note	DSPLL A: selecting the highest bandwidth allowed by the application is recommended to minimize phase deviation on input switch	[1]
☐	Note	DSPLL C: selecting the lowest bandwidth allowed by the application is recommended to minimize phase deviation on input switch	[1]

Footnotes:

[1] Recommendation is based on the frequency plan and selections in the hitless input switching assistant. Loop bandwidth is configured on the "DSPLL Configure" page of the CBPro wizard.

- A new section is included in your design report:

```
Hitless Input Switching Assistant
=================================
DSPLL A: Assistant Enabled
   Switched Externally: No
   Standards:           ITU-T G.8262 SyncE EEC Option 1/2 (± 4.6 ppm)
                        ITU-T G.812 Type II/IV (± 4.6 ppm)
                        ITU-T G.813 Option 1 (± 4.6 ppm)
   Max Freq Offset:     ±4.6 ppm

DSPLL C: Assistant Enabled
   Switched Externally: Yes
   Standards:           Other (± 15 ppm)
   Max Freq Offset:     ±15 ppm

DSPLL D: Assistant N/A
```

Version 2.27 [2018-08-10]

Si5332:

- Support Revision D
- Support encapsulated crystal packages (grade E/F/G/H)
- Support Si5332-12IX-EVB, Si5332-8IX-EVB, and Si5332-6IX-EVB encapsulated crystal EVBs
- Support multi-profile mode
    - Up to 32 profiles can be configured via up to 5 profile select pins
    - Selectable global or per-profile feature configuration to speed data entry and ensure synchronization of configuration common between profiles

Si534x/8x/9x:

- Fixed: CBProProjectSettingsExport was not including SiLab bank registers that are included in the CBPro GUI register/settings export
- Fixed: could receive export/write/OPN error regarding LOLx_INT_TIMER_SCL if fastlock bandwidth was low (or fastlock was disabled and loop bandwidth was low)
- Si5348/83/84: Fixed: on input clock selection mask, IN3/IN4 checkboxes were enabled even though they have no effect and OOF is not supported
- Si5348/83/84: new DRC error if hitless switching is enabled on PLL with IN3/4 CMOS input
- For all parts that allow mix of integer N < 10 and fractional N > 10, in certain cases the frequency planner could not find a solution when there was a mix of frequencies > Fvco(min)/20 and those that require N < 10
- Show OOF[3] disabled when ZDM is enabled
    - Set OOF_EN[3] and FAST_OOF_EN[3] to 0 and clear THR/etc settings for ZDB
    - Disable INTR mask checkbox and clear OOF_INTR_MSK[3]
- Don't allow DCO on N0 if ZDM is enabled: add DRC error if already configured in project; customize lock icon in DCO editor
- Add DRC warning if set non-zero I/O delay on N0 if ZDM is enabled

Version 2.26.0.1 [2018-06-28]

Si5332/57:

- Fixed: NVM burn with field programmer socket or wired would result in invalid NVM configuration. This bug was introduced in CBPro 2.25.2

Version 2.26 [2018-06-24]

Added Support for Si5391 (Low-Jitter, 12-Output, Any-Frequency, Any-Output Clock Generator)

- Detects and controls a SI5391A-A-EB and SI5391P-A-EB
- Can create a custom factory programmed part (Orderable Part Number)
- Can export a configuration for in-system programming using I2C or SPI
- Supports NVM burning through field programmer socket and wired to customer PCB using serial cable

Si534x/8x/9x:

- Fixed: if DSPLL C or D were used in a configuration, pin control mode on DSPLL B was ignored and register controlled mode was configured via IN_SEL_REGCTRL_PLLB
- Fixed: some older CBPro project files could not be opened on German (and possibly other) PCs; would get the equivalent of "bad data" as the error message

- Fixed: Si5340/1: if only a single input was defined and ZDM was enabled, received DRC error "must define a non-Zero Delay Mode input on DSPLL" erroneously
- Si5392/4/5/6/7: update documentation links
- Si5380/86: changes for Fpfd >= 1.024 MHz: minimum DSPLL B loop bandwidth in ZDM relaxed from 100 Hz down to 10 Hz; minimum gapped input clock frequency requirements increased by a factor of two
- Small updates to fractional P divider / gapped clock and input frequency warning thresholds based on PFD frequency and selected loop bandwidth

Si5334/35/38/55/56/57:

- Fixed: LVCMOS In-Phase format was raising an error when trying to submit an OPN
- Fixed: Si5338 NVM file conversion to CBPro project now works even if the resulting CBPro project has a frequency planner error, possibly due to ClockBuilder Desktop allowing synthesis errors. CBPro will show the DRC error(s) after opening the converted file.

Si5332:

- Fixed: Field programmer communication config dialog was not properly setting communication to I2C, it was remembering previously set mode
- Fixed: LVDS Fast power calculation was showing 0 W in design report

Version 2.25 [2018-06-04]

Added Support for Si5392/4/5 (Up to 12 Output Any-Frequency, Any-Output Jitter Attenuator/Clock Multiplier with Ultra-Low Jitter)
Added Support for Si5396/7 (Dual/Quad DSPLL™ Any-Frequency, Any-Output Jitter Attenuator)

- Detects and controls a SI5394A-A-EB, SI5394P-A-EB, SI5395A-A-EB, SI5395P-A-EB, and SI5397A-A-EB Evaluation Boards
- Can create a custom factory programmed part (Orderable Part Number)
- Can export a configuration for in-system programming using I2C or SPI
- Supports NVM burning through field programmer socket and wired to customer PCB using serial cable
- Existing Si534x project files can be converted to equivalent Si539x design using the new project conversion tool, available from the CBPro welcome screen:



- See AN1155 Differences between Si5342-47 and Si5392-97 for more information

Misc:

- Fixed: closing a popup using the down arrow can cause opening another popup not to work, instead showing the previous popup

Version 2.24 [2018-05-23]

Added Support for Si5357 (12-Output Any-Frequency Clock Generator)

- Detects and controls a Si5357 Evaluation Board (Si5357-EVB)
- Can create a custom factory programmed part (Orderable Part Number)
- Can export a Si5357 configuration for in-system programming using I2C
- Support NVM burning through field programmer socket and wired to customer PCB using serial cable

Si5334/35/38/55/56:

- Fixed: Si5338 datasheet addendum was missing output format voltage and pin 6 description was incorrect
- Fixed: EVB regulators were not in sync with output format voltage

Si5332:

- Fixed: the frequency planner could select a PFD frequency (Fpfd) outside of the maximum limit. This could only occur for configurations with input frequencies greater than 50 MHz.
- Fixed: Field Programmer could not talk to devices configured at 1.8/2.5V IO voltage
- Fixed: PLL was not being disabled for Buffered only parts
- Fixed: Register export was missing registers to switch the part between ready and active mode
- Changed default output driver format to LVPECL
- Added support for Single LVCMOS output driver format
- Added support to select from internal/external termination for HCSL driver format

Si534x/8x:

- Fixed: FOTF for Si5340/41/42/42H/44/44H/45 could give error “some outputs on the same VDD supply do not have an even common multiple within the Fdco range” when there is no issue
- Fixed: bandwidth could be set lower than needed
- Fixed: planner could give error "calculated NF, Infinity, is too large for register"
- Si5380: support phase noise estimate tool
- Make CBProFOTF1.exe the documented, primary name for Si534x/8x FOTF; allow CBProSi534x8xFOTF.exe to be run still for backwards compatibility

Misc:

- Fixed: the field programmer selector in Design Dashboard was not customized for non-Si534x/8x families when the socket was missing
- Show special message in Orderable Part Number / Phase Noise Request wizard if user has not consented to the new silabs.com data policy
- Updates to *CBPro Tools & Support for In-System Programming*
- Improved support for pre-production devices

Version 2.23 [2018-04-10]

Added support for Si5334/35/38/55A/56A, Si5338-EVB, and Si5356-EVB.

Si534x/8x:

- Fixed: high frequency outputs (require Nx<10) could not always be manually assigned to an Nx divider
- Add tooltip to explain DCO Range

Si5381/2/6 Phase Noise Estimate Tool:

- Fixed: closing CBPro without first closing the PN window would leave hung CBPro running in the background
- Do not calculate estimate if the output frequency is less than 10 MHz
- Set the maximum frequency of the input phase noise plot to be no higher than the maximum frequency of the output phase noise plot
- Update output selector items if an output is added/removed from project while the tool window is still open
- Misc. user interface

Version 2.22.1 [2018-03-28]

Si534x/8x:

- Fixed: NVM program tool could abort with “error parsing NVM file”

Version 2.22 [2018-03-27]

Misc:

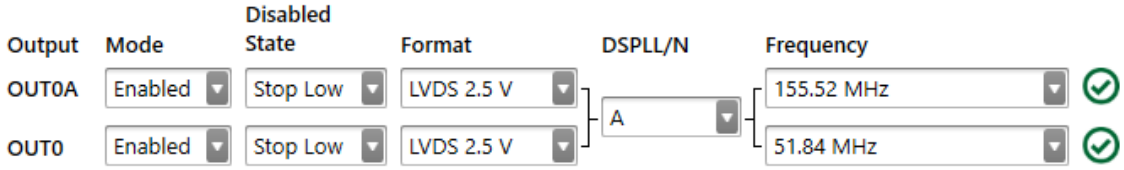
- There is a new EVB/USB driver README in C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\Drivers. Please review it if CBPro is not detecting a supported Silicon Labs Timing EVB.

Si5332:

- Register exports created by CBPro GUI Export tool, CBProProjectRegistersExport CLI, and related CLIs now include preamble and postamble required to fully reconfigure the device (via register 0x06 write).

Si534x/8x:

- Si5342H/44H: support outputs down to 100 Hz (was 8 kHz)
- Si5340/1/2/4/5: jitter optimization has been improved when DCO is enabled on a MultiSynth. When DCO is enabled, the planner priority page is no longer shown. A MultiSynth (Nx) divider that was previously integer may now have a fractional value after this change, to reduce jitter across all outputs (DCO and non-DCO).
- Si5346/47/96/97: better error message if can't calculate a frequency plan due to required resolution of dividers
- Si5380: default OLPD gain now varies depending on reference type: XTAL=1,XO=8; previously it was always 1. When using a low noise XO, increasing the OLPD gain improves the close in phase noise. This change is consistent with the default settings for the rest of the Si538x devices.
- Si5380: switch to XO as default reference for rev D
- Si5380/1/2/6: the clock output editor and frequency planner now supports discrete frequency entry and driver configuration on OUT0/0A and OUT9/9A. For example:

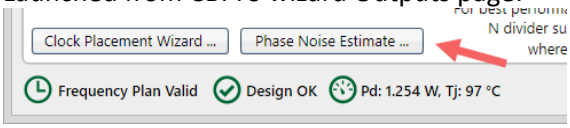


- If an Si5381/2 CEVB rev D is detected, "Open Default Plan" will set XAXB mode to XTAL
- Change Si5344 EVB sample input select mode to auto-revert

New Si5381/2/6 Phase Noise Estimate Tool:

- Supports three input phase noise data modes:
  - Jitter generation only (-200 dBC/Hz input)
  - Very high input jitter example
  - Custom PN CSV file
- Calculates RMS Jitter calculation, with configurable integration bandwidth
- Can save PDF report

- Can save plot data to CSV
- Launched from CBPro wizard Outputs page:



Improved Si5346/47 FOTF (CBProSi534x8xFOTF CLI):

- Updated preamble and postamble in DSPLL plan scripts to ensure PLL operates as expected on plan change. In prior releases, a PLL could generate wrong frequency(s) after PLL plan script write.
- LOL and OOF settings can now be configured in plan scripts:
    - LOL thresholds for a DSPLL can optionally be changed using the LOL_SET_THR and LOL_CLR_THR keywords. Decimal values are accepted. Can only be used if the base project file has "Auto Set" unchecked.
    - OOF thresholds for an input can be set using the OOF_SET_THRx, OOF_CLR_THRx (precision OOF) and FAST_OOF_SET_THRx,FAST_OOF_CLR_THRx (fast OOF) keywords, where x is the INx input number starying at 0. Thresholds can only be specified if the Enabled checkbox is set on the corresponding input. Decimal values are supported for precision OOF and integer values for fast OOF. OOF can only be changed on an input that feeds a single DSPLL.
    - Example:
      1,LOL_SET_THR,30
      1,LOL_CLR_THR,3
      1,OOF_SET_THR0,10
      1,OOF_CLR_THR0,1
      1,FAST_OOF_SET_THR0,2000
      1,FAST_OOF_CLR_THR0,1000
- Si5346/7 plan scripts now contain read-modify-write mask column. When mask is not 0xFF, read-modify-write should be performed for the register write.
    - Under certain FOTF conditions, PLL settings that share a common address/register may need to change on a per-plan basis
    - For example, LOL_SLW_DETWIN_SEL_PLLA and LOL_SLW_DETWIN_SEL_PLLB share the same register, 0x009B
    - PLL DCO frequency or target bandwidth change can affect these values
    - Writes to registers that have multiple PLL settings (bitfields) at the address therefore now have a read-modify-write mask
    - The mask is documented within the PLL plan script via comment:
      Address,Value,Mask
      # If mask is 0xFF, no read-modify-write is required. Otherwise,
      # read register value and write to device Read&~Mask + Value&Mask
    - Example:
      # Write Configuration
      0x009B,0x56,0xF0
      0x009D,0x95,0x0C
      0x00A9,0x35,0xFF
      0x00AA,0x0A,0xFF
    - The first two writes require read-modify-write. The last two do not.
    - Only Si5346/7 FOTF plan scripts will contain the mask. The full config script does not. Other parts, like single PLL Si5345, do not include the mask at all.
- DSPLLx-Register-Script-All-Plans.csv files are no longer created by the tool because of more complex preamble/postamble. If any file is found in the output folder, it is removed to ensure existing users of tool do not try to use the out-of-date script.

- Device revision B is no longer supported by the FOTF tool. The updated preamble and postamble required to guarantee configured output frequency on PLL plan change is not supported by Si5346/7 revision B. If you try to run the CBProSi534x8xFOTF CLI against a revision B project file, the tool will abort with an error.
- The samples, CLI manual, and programming overview deck have been updated for recent changes (mask,LOL,OOF)

Read-Modify-Write Mask is Supported by Register Write Tools:

- The EVB GUI File->Write Register File to Device feature now supports optional read-modify-write mask, allowing new Si5346/7 FOTF scripts to be tested
- Mask is after data; e.g.
  Address,Data[,Mask]
  Spaces and tabs can also be used to separate fields
- CBProDeviceWrite CLI --registers mode also can handle the mask field
- Example for Si538x/4x:
  - ```
    CBProDeviceRead  --settings DESIGN_ID0
    Searching for EVBs/FPs ...
    Reading from device ...
    Location     Type  Setting Name  Decimal Value  Hex Value
    -----------  ----  ------------  -------------  ---------
    0x026B[7:0]  R/W   DESIGN_ID0    53             0x35
    ```
  - mask1.txt:
    `0x026B 0xFF 0x0F` *<- Only write lower nibble of register; upper nibble is kept as is and data in second column is ignored when masked*
  - ```
    CBProDeviceWrite --registers mask1.txt
    Searching for EVBs/FPs ...
    Writing registers on Si5341A Rev D EVB (with validation) ...
    ```
  - ```
    CBProDeviceRead  --settings DESIGN_ID0
    Searching for EVBs/FPs ...
    Reading from device ...
    Location     Type  Setting Name  Decimal Value  Hex Value
    -----------  ----  ------------  -------------  ---------
    0x026B[7:0]  R/W   DESIGN_ID0    63             0x3F
    ```

New CBProRegistersToSettings CLI:

- Breaks out device register values by named setting (bitfield).
- For example, if the device is Si5345 Revision D and regs.txt contains:
  0x0302,0x00
  0x0303,0x00
  0x0304,0x00
  0x0305,0x80
  0x0306,0x05
  0x0307,0x00
  0x0308,0x00
  0x0309,0x00
  0x030A,0x00
  0x030B,0x80
- ```
  CBProRegistersToSettings --part si5345 --rev d --infile regs.txt:
  Location      NVM   Flag  SettingName  DecValue     HexValue
  ```

```
------------  ----  ----  -----------  -----------  -----------
0x0302[43:0]  User  R/W   N0_NUM       23622320128  0x580000000
0x0308[31:0]  User  R/W   N0_DEN       2147483648   0x80000000
```

- Text, CSV, and HTML output format is supported using the --format option

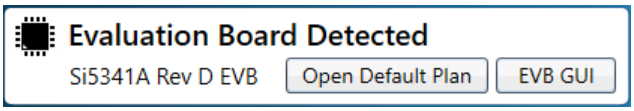
Version 2.21 [2018-01-19]

Misc:

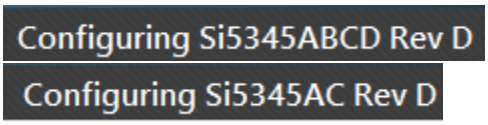
- Fixed: EVB detection could fail on Windows XP

Si534x/8x:

- Fixed: when exporting or writing a free run only project, could get error "input clock select mode must be defined"
- Fixed: Si5349/81/82: in ZDB mode, Fpfd(min) of 1 MHz was not being enforced
- All bandwidths forced to be Fpfd/40 or less; previously fastlock could be up to Fpfd/20
- Based on Px divider, Fpfd, & ZDM state, apply bandwidth range restrictions on fastlock and holdover exit bandwidth the same as loop bandwidth
- Include device grade in EVB labels in all cases:



- For select configurations, the wizard header now reflects possible OPN grades based on Fout(max) and possibly fractional MultiSynth state:

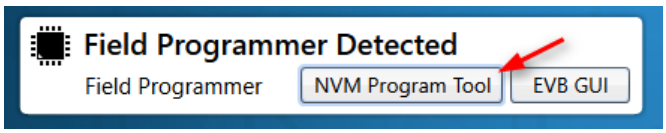


Si5332:

- Fixed: Changing XAXB input mode was not updating its use to PLL and causing a DRC error
- Fixed: register and setting exports were displaying 2 byte address instead of 1 byte address

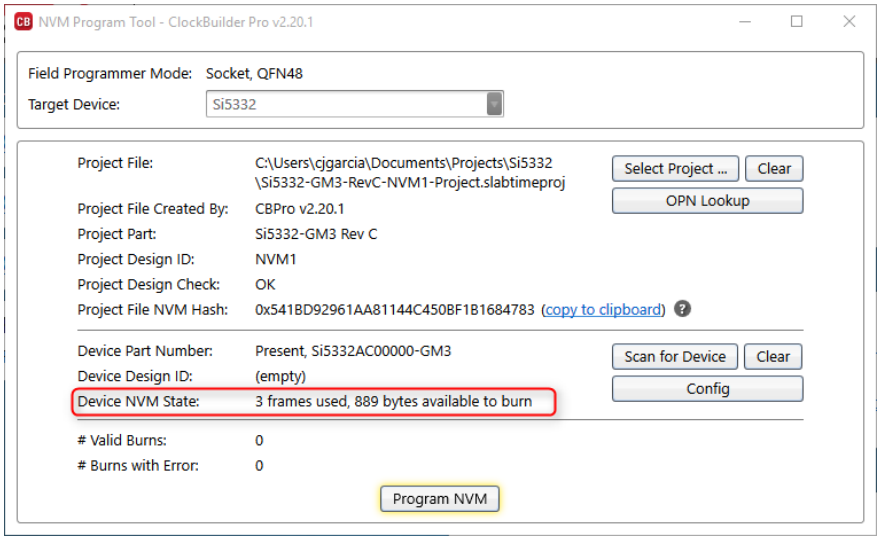
New Si5332 NVM Program Tool:

- Device to program can be:
  - In field programmer socket (Si5332-32SKT-DK, Si5332-40SKT-DK, Si5332-48SKT-DK)
  - Wired to customer PCB using serial cable
- Launched from CBPro Welcome page, just like when targeting Si538x/4x



- Scan reports on the number of non-volatile memory frames used, available free memory, and the part's OPN
- Note: if the Field Programmer's firmware needs to be upgraded to support Si5332, a dialog will prompt the user to upgrade the firmware upon programming a DUT's NVM. If upgrade fails, there is a new tool in CBPro's Start menu Misc folder to re-flash a Field Programmer with corrupt firmware. This would only occur if user disconnects field programmer during the one time firmware upgrade process.

- Example:



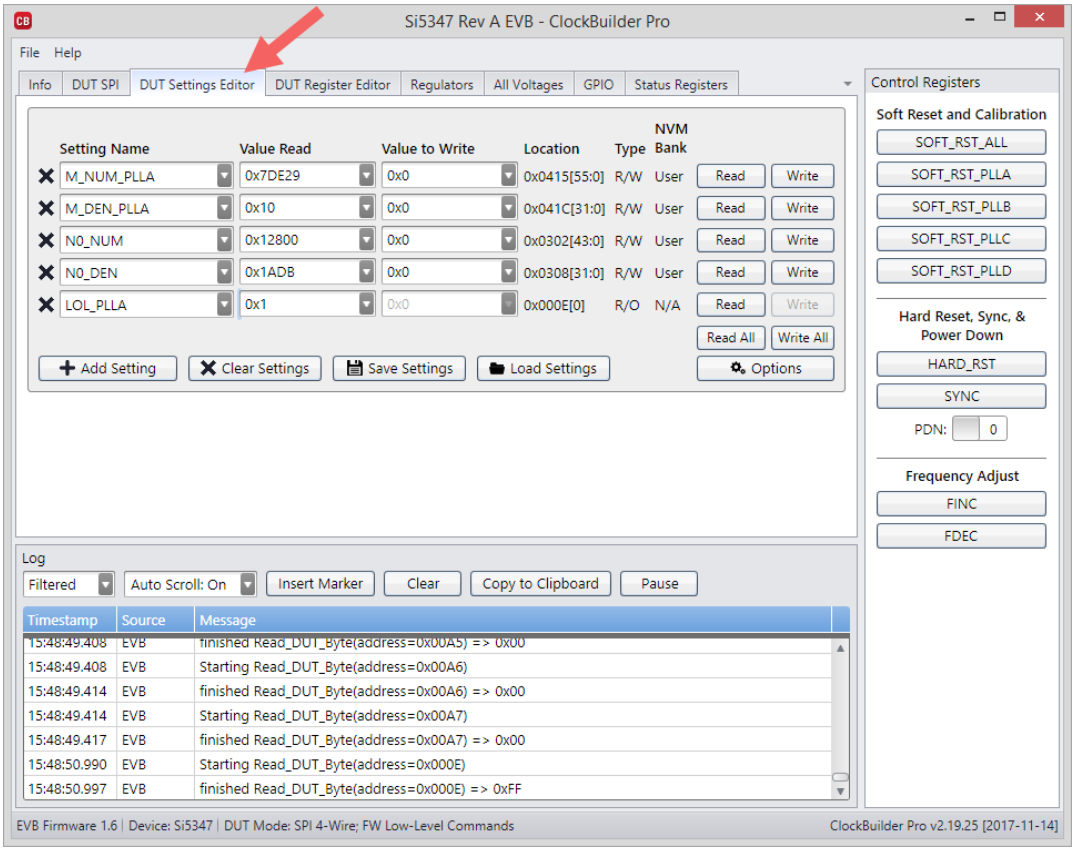
Version 2.20 [2017-11-21]

Misc:

- Fixed: rare crash when trying to select save filename in export, etc.
- Fixed: CBProMultiProjectExport.exe CLI was not creating delta full reconfigure scripts even though it was documented to do so
- The USB driver now fully supports Windows 10 UEFI Secure Boot PCs via a certified driver that is installed on such PCs. Non-secure boot PCs will continue to use the existing driver.

New Settings Editor in EVB GUI:

- Read and write registers based on their setting names (aka bitfields)
- Supported on Si5332, Si535x, and Si538x/4x: EVB or field programmer
- New tab next to Register Editor



- CBPro automatically saves your current settings group to its preferences, keyed off of part number. So when you relaunch, they will be reloaded. But you can also save a group to a text file using the “Save Settings” button, and later restored using the “Load Settings” button
- Example saved settings file:

```
# Si5347 Settings
# Saved by ClockBuilder Pro v2.19.25 [2017-11-14] EVB GUI Settings Editor
# Saved on 2017-11-14 15:53:05 GMT-06:00
SettingName,Location,Type,NVM,ReadValue,WriteValue
M_NUM_PLLA,0x0415[55:0],R/W,User,0x7DE29,0x0
M_DEN_PLLA,0x041C[31:0],R/W,User,0x10,0x0
N0_NUM,0x0302[43:0],R/W,User,0x12800,0x0
N0_DEN,0x0308[31:0],R/W,User,0x1ADB,0x0
LOL_PLLA,0x000E[0],R/O,None,0x1,0x0
```

Si5332:

- Fixed: adding spread spectrum pin could cause error, preventing the plan from being calculated
- Fixed: Spread Spectrum not working in grades C and D Orderable Part Numbers (OPNs)
- Modified Output Enable (OE) universal hardware pin to be OE bar
- Added support for Si5331 CEVB

Si51218:

- Fixed: mux was configured incorrectly for two clock outputs

Si538x/4x:

- Fixed: in rare cases, enabling outputs on old project files could crash CBPro

- Fixed: if DCO step size was the same as range, design report would list output as "DCO not supported on this output"; device settings were still OK
- Fixed: exporting firmware boot record or upgrading firmware on Si5383/4 was not working on 32-bit Windows
- Fixed: clicking the input priority arrow very fast could crash CBPro
- The NVM Program Tool now validates volatile writes before initiating burn; if mismatch, burn is aborted and user is notified of differing registers
- Si5381/2/6: Grade A (external) reference frequency now selected via pulldown, limited to 48.0231 MHz and 54MHz
- Si5348/83/84: the setting (register bitfield) name for REF priority was changed from IN3_PRIORITY_PLLx to REF_PRIORITY_PLLx
- Si5346/47/48/83/84: the following settings were removed from exports, design reports because they do not apply to these devices:
    - 0x0240[1] MXAXB_FSTEP_DEN
    - 0x0240[0] MXAXB_FSTEP_MSK
    - 0x0241[43:0] MXAXB_FSTEPW
- The frequency planner for Si5340/1/2/4/5 and Si5381/2/6 has been improved to allow integer N<10 across a wider range of output frequencies. Previously this set out outputs:
    - 20 MHz
    - 40 MHz
    - 60 MHz
    - 140 MHz

  would not be placed on single N divider. Now they are, via automatic or manual N divider assignment

Updates for pre-release devices.

Version 2.19.3 [2017-09-25]

Si5382:

- Fixed: CBPro could crash on free-run only wizard page

Version 2.19.2 [2017-09-25]

Si5332:

- Fixed: DRC error was taking into account unused clock outputs in VDDO check

Version 2.19 [2017-09-24]

Added support for **Si5381/82** 12-channel Multi-DSPLL Wireless Jitter Attenuating Clocks

Added support for **Si5386** 12-channel, Any Frequency, Wireless Jitter Attenuating Clock

Misc:

- Fixed: when a project file was opened by double clicking it from Explorer, Outlook, etc. the filename was not reused when you later re-saved, created a design report, etc.

Si538x/4x:

- Remove 0x0402 and 0x0502 addresses from exports on select parts, where the register values never vary from factory programmed values, are never modified by CBPro, and would never be reprogrammed by customers.

- Small modification to BW0-BW5 DSPLL coefficient calculation. Generally will not result in operational bandwidth change on device, just +-1 change in any one BW0-BW5 setting value. I.e. the “actual bandwidth” value reported in the CBPro design report will normally not change as a result of this update.

Si5332:

- Fixed: changing output format to LVCMOS was not updating properly the output frequency range
- Fixed: Output skew page was incorrectly displaying “ns” instead of “ps” for the offset
- Fixed: frequency planner could select N divider outside range in certain cases, resulting in visible Design Rule Check error
- Added part grade description to OPN Wizard

Version 2.18 [2017-09-17]

Si5332 Support Added (6/8/12-Output Any-Frequency Clock Generator):

- Detects and controls a Si5332 Evaluation Boards (Si5332-12EX-EVB, Si5332-8EX-EVB, Si5332-6EX-EVB).
- Can create a custom factory programmed part (Orderable Part Number)
- Can export a Si5332 configuration for in-system programming using I2C

Updates for pre-release devices.

Version 2.17 [2017-09-11]

Misc:

- Add new --noscan-in-fp-registers-mode option to CBProDeviceRead and CBProDeviceWrite CLIs. Communication with the device using the field programmer is normally verified before an operation by reading fixed identification register(s) such as PN_BASE on Si538x/4x. Specifying this option will disable this behavior when --registers mode is used.

Si538x/4x:

- Fixed: Si5342H/44H: in register export scripts, don't include 0x0540=0x00 register write (OLB_TM_OUT_ZERO=0) in postamble if DCO mode is enabled. This needs to remain 0x01 (OLB_TM_OUT_ZERO=1) to disengage the other loop. This bug was introduced in CBPro 2.13.3.
- Fixed: when targeting device using field programmer, writing a rev B project file would yield an error due to locked SiLab register being written and failed read back validation
- Fixed: on rev D+, INIT_LP_CLOSE_HO[_PLLx] configuration bit is now set to 1 when either ramped exit from holdover option is selected in CBPro DSPLL Configure page. Previously, it would have been 0. Without this setting, if the DSPLL first initializes with no input clocks, enters free run, and later an input is available, the DSPLL will not ramp when exiting free run.
- Fixed: if you wrote a design from the CBPro wizard without EVB GUI open, launched the EVB GUI, and then ran the power measurement compare, it complain saying must write project.
- Remove ID settings refresh button from field programmer EVB GUI; use scan instead
- On rev D+, support 1/16 ppm resolution on precision OOF thresholds through writing of OOFx_CLR_THR_EXT, OOFx_TRG_THR_EXT settings
- Add text to gapped clock tooltip: "A valid gapped clock must have a minimum frequency and clock cycle density as specified in the datasheet."
- Raise Fpfd(min) when Zero Delay Mode is enabled from 64k to 128k
- OOF improvements:
    - Editor enforces that OOF clear threshold must be <= trigger threshold

    - New DRC error if OOF clear threshold must is > trigger threshold; therefore existing projects that violate new editor rules will be flagged with error
- Only include N_FSTEP_MSK in exports/reports on devices that do DCO on Nx (40/41/42/44/45, not 42H/44H).
- Improve Zero Delay Mode (ZDM) phase alignment at low PFD frequencies by changing how loop gain coefficients are calculated
- DUT Dump feature in EVB GUI supported in field programmer again

CBProSi534x8xFOTF CLI:

- Fixed: the tool ignored the plan(s) for N4 divider. I.e. the --plans-n4 option was being ignored.
- For Si5340/41/42/42H/44/44H/45, the frequency planner in FOTF mode now optimizes for lowest jitter even if that means that no single N divider is integer.

Updates for pre-release devices.

Version 2.16.1 [2017-07-19]

Si538x/4x

Fixed: when creating a new Si5348/83/84 design, IN3/4 CMOS only inputs were auto assigned to DSPLL A&C; these inputs are DSPLLD only

Version 2.16 [2017-07-18]

Si535x

Fixed: Incorrect pin mux configuration for Si5351A

Si538x/4x

Si5340/41/46/47 Stuck Divider Fix:

- During power up or upon hard reset, some Si5340/41/46/47 devices may, on rare occasion, see an unusual clock divider failure resulting in output clocks not being generated. Once a device has successfully generated clock outputs, they will continue running without issue. Although the failure mechanism is random, Silicon Labs has not observed successive failures in tests run over many parts. Silicon Labs has observed that in several devices cycled with a hard reset more than a million times, output clock failure rates can be seen in rare instances (a few hundred times). Multiple workarounds in case of clocks not being generated have been identified and are detailed below.
- Fix: Orderable Part Numbers (OPNs) created by CBPro 2.15.6+ will have a baseline register changes to address the issue
- Fix: Register script exports generated by CBPro (wizard,CLIs) have fix via update to programming preamble

Si5342/42H/44/44H/45/46/47/48/83 Precision & Fast OOF Disabled Exit From Holdover Fix:

- If both precision and fast OOF were disabled for an input clock and holdover history was valid the device, exit from holdover would not occur on clock recovery
- Example sequence showing issue:
    - Lock the device — all is OK
    - Remove the clock — all is OK; OOF, LOS and LOL are all asserted
    - Put the input clock back — OOF, LOS, HOFRB are negated, LOL is asserted, the input and output are not locked
    - Issue a soft reset — all is OK
- Fix: if both precision and fast OOF were disabled, CBPro now:
    - Sets OOF_CLK_DIS[in] and OOF_DIV_CLK_DIS[in] to 1 if input is not enabled (change)

- Sets OOF_ON_LOS[in] if input is not enabled OR precision OOF is enabled OR fast OOF is enabled (new setting; change so that device does not assert OOF with LOS)

Si5342H/44H N_PIBYP Fix:

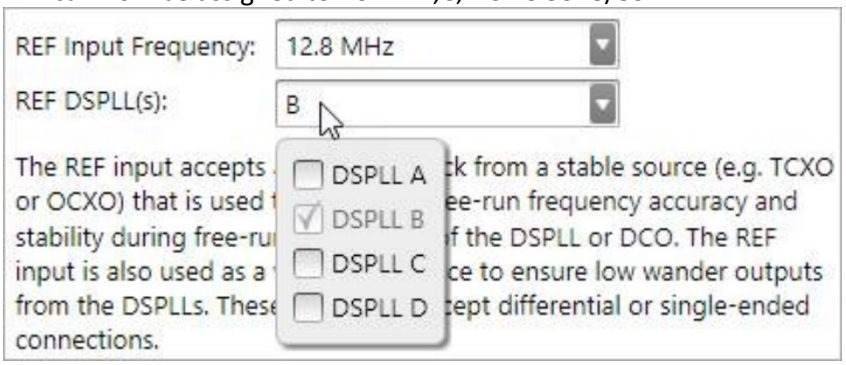
- When DCO mode was enabled and N0 divider was integer, N_PIBYP[0] would have the wrong value.
- If DCO mode was enabled, N0 divider was integer, and N_PIBYP[x] was incorrectly set, then frequency plans approaching the upper frequency limit could yield no output clock.
- Fix: N_PIBYP[x] set to 1 if Nx is integer and 0 if Nx is fractional.

Other Bug Fixes:

- Fixed: OUT1_DIV2_BYP (Si5342H/44H) and OUT3_DIV2_BYP (Si5344H) were not included in design reports and settings exports; the correct values were reflected in register exports and NVM images, however, so no customer configuration issues
- Fixed: Si5342H/44H: was not always supporting R bypass for high speed outputs when manually assigned to an N divider
- Fixed: Si5383/84: if the project used fixed host I2C address mode, the address was not editable until mode was toggled
- Fix rare crash when close NVM burn tool window

Misc:

- Si5340/41/42/44/45 Rev D: Nx_HIGH_FREQ bit is now set if a MultiSynth (Nx) divider value is less than 10. This bit is in 0x0A14[3], 0x0A1A[3], 0x0A20[3], 0x0A26[3], and 0x0A2C[3]. This improves clock stability for high MultiSynth frequencies.
- Changed the default ramping for new designs to ramped exit from holdover only. This is the recommended setting when switching between input clocks that differ in frequency by less than 10 ppm. The text has been improved for available options.
- Rev D: new checkbox on PLL page to enable or disable preserve holdover history. This controls the HOLD_PRESERVE_HIST[_PLLx] setting. Preserve holdover history should be turned OFF if clock switching between two input clock that are different in frequency by more than 10 ppm.
- Improved spur avoidance in frequency planner.
- New LOS threshold “set for me mode”. This is the default for new designs. Silicon Labs recommends checking this when hitless switching is enabled to ensure optimal performance.
- Miscellaneous Design Rule Check (DRC) changes
- REF can now be assigned to DSPLL A,C,D on Si5348/83



- GRADE, PKG_ID, OPN_IDx, and OPN_REVISION are now included in datasheet addendums, matching the value programmed on the device at the factory.
- Updates for pre-release devices

Version 2.15 [2017-05-12]

Si535x:

- Fixed: OE control was not being cleared when exporting
- Fixed: Outputs where being powered down when selecting Disabled
- Fixed: No solution plan was showing as empty plan in design report instead of displaying error.

Si538x/4x:

- Si5348/83/84: show DSPLL B(REF) options (bandwidth)
- Si5383/84:
    - Fixed: Fout(max)=33.554432MHz on OUT6 when OUT5=1Hz was not being enforced; would allow entry, but any real/virtual DUT write such as orderable part number creation, register export, or EVB write would generate error due to R divider range being exceeded
    - Power estimate improvements

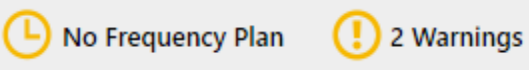
ClockBuilder Pro Field Programmer:

- CBProDeviceWrite, CBProDeviceRead Command Line Tools (CLI)
    - New: supports in-socket read/write
    - New: supports Si5383/84 via the new --family argument (--family si538x4x or –family si538x4xfw)
    - The --family argument is now required when targeting a PCB via I2C or SPI serial connection except for CBProDeviceWrite --project mode (family can be inferred in this use case)
- CBProSi534x8xFirmwareDownload CLI now supports the field programmer in socket mode
- NVM Programming Tool:
    - Now supports Si5383/84 flash programming, in-socket or in-system (wired to PCB)
    - The button to launch the tool on the welcome screen, previously labeled “NVM Burn Tool”, is now labeled “NVM Program Tool”
    - Improvements for other Si538x/4x (non-firmware) devices:
        - Reporting of full part number of detected device
        - Explicit design rule check results performed on project selection
        - Improved organization/layout
- The EVB GUI now supports the Si5383/84 via field programmer, using new LGA56 field programmer socket or in-system (wired to PCB)
- The CBPro wizard now supports in-socket or in-system (wired to PCB) write to DUT; previously the dashboard forced the field programmer to assume wire mode

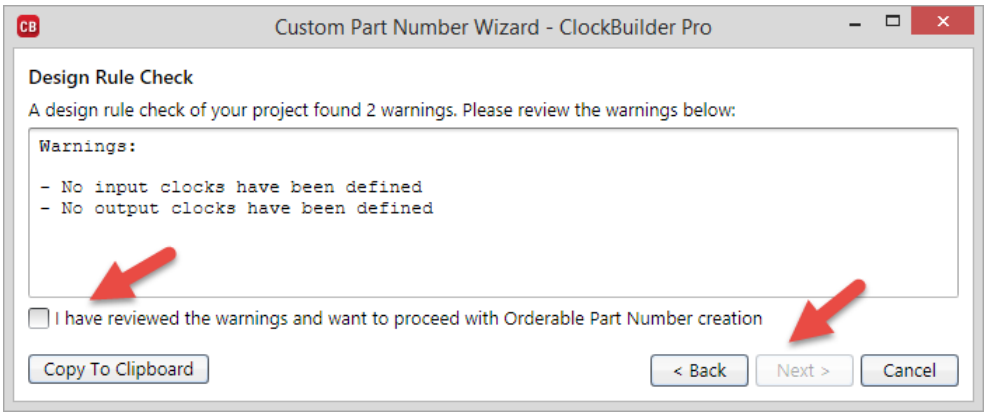
Version 2.14 [2017-04-21]

General:

- You can now create “no plan” projects when a device supports in-system programming. For example, on Si5351A and Si5345 you don’t have to define an input or an output to create an OPN or export the design. DRC warnings are generated instead of errors.



- The OPN wizard now requires you to review any DRC warnings present and acknowledge them by clicking a checkbox before continuing:



- Fixed rare error "cannot set Owner property to a Window that has not been shown previously" when opening project with frequency plan change
- When exporting file from dashboard, device revision is included in the default filename
- Updates for pre-release devices

Si535x:

- Fix bug where the pin mux mapping between C0/C1 and P1/P2 was switched for Si5350B/C
- Improved frequency planner to allow the use of both PLLs when it cannot find a solution and all outputs share the same feature

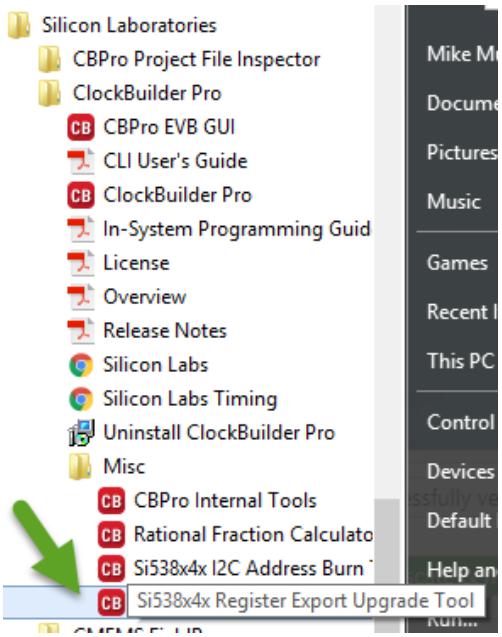
Si538x/4x Register Export Improvements:

- Improved programming reliability for the following conditions:
  - Writing a configuration script too slowly can cause a faulty VCO calibration that may trigger a LOL signal (Si5342/44/45/48, Si5342H/44H, and all Si538x) operating over temperature.
  - If a new configuration is loaded within 300 msec of reset or within 300 msec of loading a previous configuration, the device may still be running its calibration sequence, possibly leading to a faulty VCO calibration that may trigger a LOL signal.
- The changes described below ensures programming functions as intended under all conditions regardless of how slowly the configuration script is written or how recently another configuration has been loaded.
- Register export changes:
  - Si5342/44/45/48, Si5342H/44H, and all Si538x: added register 0x0540 writes to preamble/postamble
  - All devices: added 300 msec delay after preamble to export scripts and real DUT writes for all devices (i.e. done on EVB and field programmer). In export scripts the delay is added as a comment.
  - Added comment blocks to register export scripts breaking preamble, configuration, and postamble into sections
- Example of new export script:

```
# Start configuration preamble
0x0B24,0xC0
0x0B25,0x00
0x0540,0x01
# End configuration preamble
#
# Delay 300 msec
#    Delay is worst case time for device to complete any calibration
#    that is running due to device state change previous to this script
#    being processed.
#
# Start configuration registers
0x000B,0x68
```

```
0x0016,0x02
…
0x0B57,0x0E
0x0B58,0x01
# End configuration registers
#
# Start configuration postamble
0x0514,0x01
0x001C,0x01
0x0540,0x00
0x0B24,0xC3
0x0B25,0x02
# End configuration postamble
```

- New “Si538x/4x Register Export Upgrade Tool” is available to add 0x0540 write, delay comment, and section comments to an existing register export
    - CSV and C header file files supported
    - Launched from Start Menu:



    - Does in place edit, creating backup of original

Si5348/83/84:

- 83/84: Fixed: an N divider could be selected outside the restricted DCO range in 1pps mode; you would get a plan check DRC error if this occurred
- 83/84: Fout(max) now set to 685 MHz on DSPLL D if 1pps input mode
- 83/84: rapid lock calculation update
- Si5383 sample design updated: DSPLLA and C set to 10Hz with 100 Hz fastlock
- Si5384 sample design added
- All: changed default nominal and fastlock bandwidth for new designs on DSPLL A/C/D from 100/1k to 10/100 Hz
- All: new DRC when DSPLL A, B, or D bandwidth is >= DSPLLB bandwidth. Example:
  Because DSPLL A,C bandwidth is equal to or higher than DSPLL B bandwidth, the stable clock connected to the REF input will not be used as a jitter / wander reference for DSPLL A,C. It will, however, continue to function as the free run / holdover reference.

Si538x/4x Misc:

- Fixed: could not load very early (old) Si5348 project files that did not use all PLLs
- Fixed: if Zero Delay Mode (ZDM) was enabled, the planner could place even common multiple related outputs on the ZDM divider even though the divider range could not support this, leading to confusing planner error. For example, if the ZDM output was 64kHz and there was a 400 MHz output, the planner would try to put these both on N0 even though the N divider range would not support this.
- Don't add hitless switching performance DRC if only 1 input clock on PLL
- Improved silab bank burn sequence used by I2C Address Burn tool
- File->Write Register File now detects “Delay XXX” comments in register file and pauses, where XXX is in milliseconds. For example:
  # Delay 100 or
  # Delay 100 msec

Version 2.13.0.1 [2017-03-27]

Si535x:

- Fixed: bug where the pin mux mapping between C0/C1/C2 and P0/P1/P2 was switched for Si5350B/C

Version 2.13 [2017-03-03]

Add support for Si5383/84, a network synchronizer supporting 1 PPS to 750 MHz inputs.

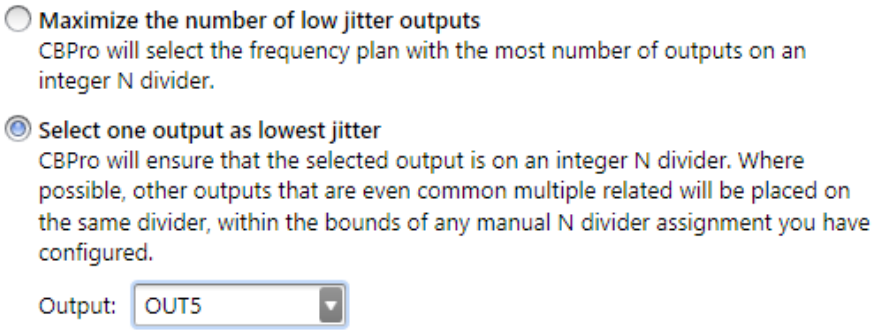
Export Improvements (All I2C/SPI Configurable Devices):

- Fixed: the multi-project export GUI was not creating per-project register write scripts and setting dumps
- Added a copy project option to multi-project export GUI and CLI. For example, if you do multi-project export on 4 project files, P1-Project.slabtimeproj through P4-Project.slabtimeproj will be created.
- Added option to create C code register config scripts to the multi-project export GUI (this was already in the CBProMultiProjectExport CLI).
- Multi-project export now handles projects that write different settings. If a register is not written (not defined and a don't care) by one project but is defined by another, the value cell will be empty for the project(s) that do not define the register. These empty cells will not count towards the Varies computation. Previously multi-project export would fail with an error under these conditions.
- Multi-project export now creates delta register write scripts in addition to full configuration scripts for each project, similar to what the CBProSi534x8xFOTF CLI creates. Each delta script includes the programming pre-amble sequence, the register writes that vary between any one project, and the post-amble sequence. This provides a more efficient way to switch between configurations using the following workflow:
  - Device power up or reset
  - Write a full configuration write script (P*-Registers-Script.txt)
  - Write any delta update configuration write script (P*-Registers-Script-Delta-Only.txt)

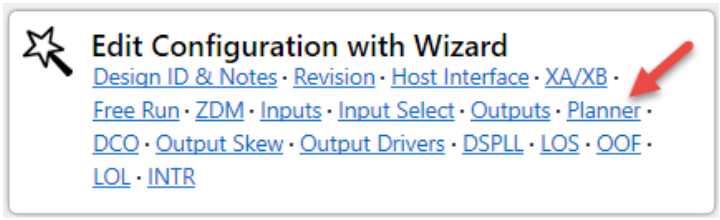
  All multi-project export samples, user manuals, and the training presentation bundled with CBPro have been updated to discuss this.
- Updated the CLI user guide, in-system programming overview, and samples to reflect these changes.

Si538x/4x:

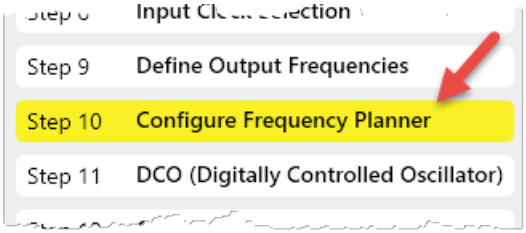
- New frequency planner priority page added to wizard for Si5340/41/42/42H/44/44H/45 projects
  - Allows you to select an output to be lowest jitter and guaranteed to be placed on an integer MultiSynth:



- Getting to the new page from the dashboard:



- From the step menu:



- Changed the threshold for "hitless switching performance may not meet datasheet specification due to Fpfd less than XXX" DRC from 64kHz to 1MHz
- Si5348: removed OLB_HO_FORCE (and associated FIXREGS) from design report, exports: never needs to be written on PLLB since free run only mode is not supported on PLLB
- NVM burn tool improved:
  - Now reports on:
    - CBPro version that created the project file
    - A unique hash (similar to a checksum) for the user NVM bytes that will be burned. This is useful to create a fingerprint of a project's resulting device configuration.
    - Cumulative # good/bad burns since the tool was launched
  - If the project file has a DRC error or other error, this is now immediately reported on instead of having to wait until the "Burn NVM" button is pressed
- EVB sample projects updated for Si5341/46/47

Misc:

- EVB GUI no longer does device reset detection polling when the SPI, I2C, or register editor tabs are selected
- Updates for pre-release devices

Version 2.12.1 [2016-12-15]

Si538x/4x:

- Fixed: The EVB GUI status registers were not properly customized for the target device when using the CBPro Field Programmer.

Version 2.12 [2016-12-12]

Si5350/51 Support Added:

- Detects and controls an Si5350/51 Evaluation Board (Si535X-B20QFN-EVB). EVB control is not supported on Windows XP.
- Can create a factory programmed part (Orderable Part Number)
- Can export an Si5351 configuration for in-system programming using I2C

Si538x/4x:

- Fixed: 1 Hz outputs on Si5348 could be relocated by the clock placement wizard. Also, it might relocate the related cascade output or assign an output to the cascade if it was not being used.
- Fixed CBProProjectEdit, CBProMultiEditAndExport, CBProSi534x8xFOTF CLI bugs:
    - Bandwidth value in m (milli) were being mapped to M (mega). CBPro now strictly treats bandwidth m as 1e-3 in edit files. In clock frequency edits, m continues to map to 1e6.
    - Setting a clock to Disabled was not working
- Fixed: Fvco was not always constant in Si5347 FOTF, causing Nx divider value written for a plan to be off
- Fixed: on Si538x/4x, CBProDeviceWrite CLI in --project mode was always setting IO_VDD_SEL to 1 when writing to a DUT via the field programmer, ignoring the setting in project file; this would cause errors when writing a project with I/O Power Supply option set to VDD(Core)
- Fixed: DSPLL holdover timing text was clipped on rev D
- The Si5340/41/42/42H/44/44H/45 frequency planner further optimizes for reduced jitter by optimizing the values of fractional N dividers
- New DRC warning on Si5340/41/42/44/45 if the DCO range is greater than 350 ppm

New CBProDeviceRead Command Line Tool:

- Reads device registers and associated named settings (aka bitfields) from an EVB or the CBPro Field Programmer (FP). Has three modes of operation:
    - Read one or more named settings you specify on the command line (--settings option). Reads are done at the register level, but output is per-setting.
    - Read one or more registers you specify either on the command line (--registers option). In this mode, no mapping to setting names is done: you get back a simple register address, value list.
    - Read all read-only and read-write settings on the device (--all option). Reads are done at the register level, but output is per-setting.
- Supports Si538x/4x, Si535x, and Si512xx EVBs. Field programmer support is currently limited to Si538x/4x devices.
- Examples:

```
C:\> CBProDeviceRead.exe --quiet --settings PN_BASE DEVICE_REV

Location      Type  Setting Name  Decimal Value  Hex Value
------------  ----  ------------  -------------  ---------
0x0002[15:0]  R/O   PN_BASE       21317          0x5345
0x0005[7:0]   R/O   DEVICE_REV    3              0x03
```

```
C:\> CBProDeviceRead --all --quiet --format csv

Location,Type,SettingName,DecimalValue,HexValue
0x0000[3:0],R/O,DIE_REV,5,0x5
0x0002[15:0],R/O,PN_BASE,21317,0x5345
0x0004[7:0],R/O,GRADE,0,0x00
0x0005[7:0],R/O,DEVICE_REV,3,0x03
...
0x0B4A[4:0],R/W,N_CLK_DIS,0,0x00
0x0B57[11:0],R/W,VCO_RESET_CALCODE,270,0x10E


C:\> CBProDeviceRead.exe --quiet --registers 0x0002 0x0003 0x0005

Address  Decimal Value  Hex Value
-------  -------------  ---------
0x0002   69             0x45
0x0003   83             0x53
0x0005   3              0x03
```

Misc:

- Updated in-system programming training available on the Welcome screen
- Updates for pre-release devices

Version 2.11.1 [2016-10-26]

Fixed: on Windows XP, project files could not be opened.

Version 2.11 [2016-10-24]

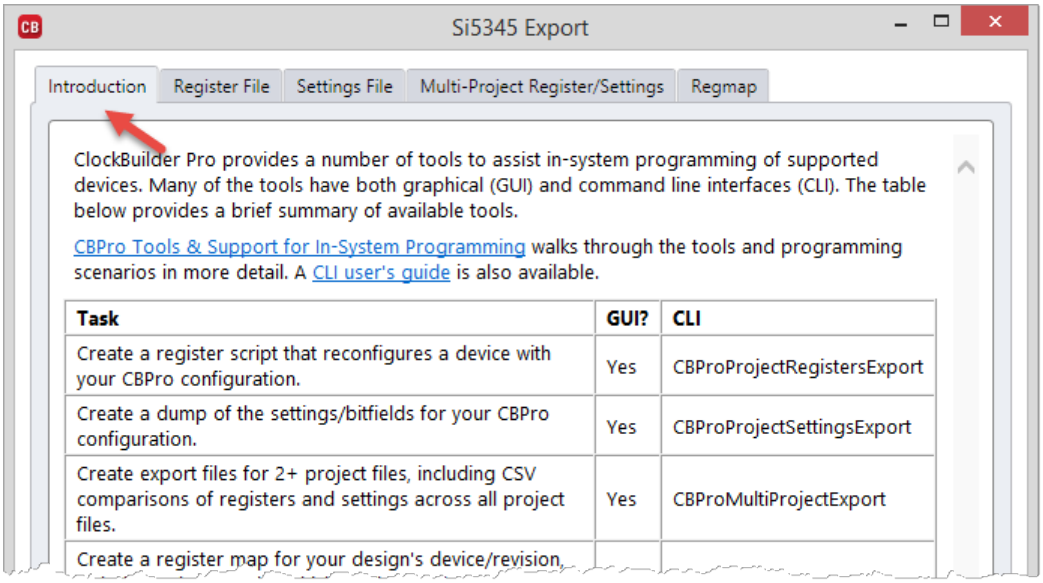
General Changes

Command Line Tools:

- New CLI, CBProMultiEditAndExport, that combines the features of CBProProjectEdit and CBProMultiProjectExport into a single tool:
    - You define a base project file
    - You define alternate clock configurations in the form of simple text file(s) (like FOTF tool)
    - You run this tool to create new (edited) project files and export files for both the base project file and created project files
    - Unlike FOTF tool, the frequency plan for each is independently solved
    - So this helps automate creating clock variations of a project in situations where the FOTF tool does not make sense – such as wanting optimal Fvco for each plan -- or is not supported (Si535x, Si5348, etc)
- More and improved CLI samples in C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\CLI\Samples
- The individual user guides for each CLI are also now copied to C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\CLI\Docs
- Brand new training deck, *CBPro Tools & Support for In-System Programming,* walks through common in-system programming scenarios/workflows and provides an overview of related tools
- Updated the CLI user manual
- Both are available through on CBPro Welcome screen and the Windows Start Menu

Misc:

- Don't allow draft datasheet addendum to be created if there are DRC errors
- The Export GUI now has an intro tab that is customized to the current part. It briefly describes available export GUIs and CLIs



- Updates for pre-release devices

Si538x/4x Family Changes

Misc:

- Fixed: if a clock frequency expression had an error and the clock was then marked Unused, further edits to unrelated clocks might not be accepted
- CBPro no longer allows an unconfigured clock to be used in a frequency expression
- Si5380: added 921.6, 460.8, 230.4, and 115.2 MHz to supported output frequency list
- GRADE (0x0004[7:0]) & TOOL_VERSION (0x0006[23:0]) DUT settings are no longer included in rev D register and settings exports; these are read only

Command Line Tools:

- Fixed: CBPro device write and firmware download CLIs – CBProDeviceWrite.exe and CBProSi534x8xFirmwareDownload – did not parse --io-voltage decimal in US-centric mode on non-US systems, causing disconnect to user manual
- CBProSi534x8xFOTF CLI:
    - Fixed: tool would fail on 40/41/42/42H/44/44H/45/80 if an output had been manually assigned to an N divider and then set to Unused
    - 41/45 mode now forces N_PIBYP[x] bit to 0 in base config and register script if an N divider is doing FOTF. This ensures that N_PIBYP remains fixed across the base and all plan scripts (and is therefore not included in any plan scripts)
- Project edit and FOTF plan files can now specify HOBW to update exit from holdover bandwidth; this is required if OLBW has been specified and ramping has been disabled

EVB GUI:

- Improved memory footprint by decreasing the number of log message lines that are cached; this should speed up EVB GUI on most systems
- Suspend status register polling during project file, register file, and setting file writes to EVB

Version 2.10 [2016-09-07]

General Changes

Bug Fixes:

- Fixed: in datasheet addendums PDF files, the Ω character was a blob of text
- Fixed: the step pulldown menu in the wizard had "(A)" after every step

New CBProDeviceWrite Command Line Tool (CLI):

- Writes a project file, settings file, or registers file to a supported EVB
- Writes to a system board using the ClockBuilder Field Programmer via I2C or SPI
- Same effect as the EVB GUI File menu "Write XXX" tools
- Help available via CBProDeviceWrite --help

Misc:

- Change addr[x:y] bitfield callouts to little endian ordered msb:lsb. For example, 0x0302[43:0] for Si538x/4x N0_NUM.
- Text in design report and frequency plan windows can now be selected
- Allow trailing // and # comments in setting and register files that can be written using the EVB GUI or CBProEVBWrite CLI. Example:
  DESIGN_ID0,65 # Decimal value (ASCII 'A')
  0x026B,0x41 // DESIGN_ID0 = 'A'

Si538x/4x Family Changes

Bug Fixes:

- Fixed: frequency ranges in rev B output editor and rev D device grade section of design reports were incorrect on Si5340/41/42/44/45
- Fixed: Fout(min) for LVCMOS outputs for all revisions changed from 1kHz to 100Hz to match datasheet

LOS Enable Changes:

- An issue exists where a loss of input signal can cause an inadvertent DSPLL recalibration when LOS is disabled. During the recalibration sequence, a loss of output clocks from the DSPLL occurs.
- As of this release, LOS can no longer be disabled.
- If a project file is opened that has LOS disabled, you will be notified and LOS will be re-enabled.

New Hitless Switching Restrictions/Warnings:

- Zero Delay Mode (ZDM) and hitless switching results in conflicting behavior. As of this release, ZDM and hitless switching can no longer be used together.
- New DRC warning if automatic clock selection is enabled, hitless switching is enabled, and a PFD frequency is less than 64 kHz: hitless switching performance is reduced in this scenario.

Misc:

- On Si5348, set PFD_TRIM_PLLx for any DSPLL not in free run only mode
- Better Fdco selection on 47-like DSPLLs on rev D for certain designs
- VDD voltage can no longer be changed in EVB GUI; it is forced to 1.8V
- Updates for pre-release devices

Version 2.9 [2016-7-29]

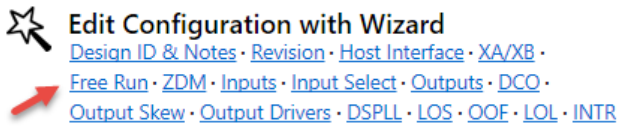
Si538x/4x Family Changes

Support Si538x/4x Revision D:

- This is the default revision for new designs
- Note you will no longer be able to create a revision B custom part number (aka OPN) without the assistance of Silicon Labs
- While you will no longer be able to create revision B custom part numbers, you can still open and edit revision B project files, and create new in-system programming exports incorporating the enhancements included in this CBPro release

New Free Run Only Mode:

- The device can now be configured to operate in free run mode. The DSPLL will operate like a clock generator in free run mode, locking to the crystal (or XO) on XA/XB
- Supported on Si5342/42H/44/44H/45/46/47/48/80
- Available on a per-DSPLL basis on Si5346/47/48
- FORCE_HOLD, FIXREGSAx, and FIXREGSDx register settings defined to support this feature
- Select via step menu or dashboard:



FOTF CLI Improved (CBProSi534x8xFOTF.exe):

- Now supports Si5340/41/42/42H/44/44H/45/80 in addition to the Si5346/47:
  - Requires you to manually assign outputs to a specific N divider
  - Alternate plans are specified on a per-N divider basis
  - Searches all desired plans for optimal Fvco
  - Creates simple register write scripts to switch a single N divider from one plan to another
  - Example included with CBPro (C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\CLI\Samples\Single-PLL-FOTF)
- Example added for Si5347 (C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\CLI\Samples\Multi-PLL-FOTF)
- Improved the user manual available via the --help option

Misc:

- Improvements to frequency planner, resulting in lower output jitter for many designs.
- New DCO Design Rule Checks (DRCs) to warn if FINC/FDEC could go beyond output frequency range
- New FIXREGSAx and FIXREGSDx register settings are included in design reports, setting exports, and register exports. These settings are NVM backed and define register address/data sequence to restore on NVM reload (such as at device reset). With FIXREGS, a DUT register that is normally not NVM backed can be essentially be made NVM backed. CBPro uses these to set the FORCE_HOLD setting in free run only mode on Si5342/42H/44/44H/45/46/47/48/80 and OUTERLOOP_DIS on Si5342H/44H based on DCO enable state. Additional FIXREGS are included in Si5346/47 to support certain factory only features.
- Improved support for pre-production devices

Bug Fixes:

- Fixed: on Si5348, DSPLL LOL gain factor could be miscalculated on DSPLL A/C/D
- Fixed: CBProSi534x8xFOTF command line tool would fail to export if an output had been assigned to a DSPLL previously, and then is marked Unused
- Fixed: 41/45 DCO report mislabeled Nx_DEN as Nx_NUM
- Fixed: if an existing project is opened that has unsupported output driver mode selected due to Fout >= 1.5 GHz, fixing the mode would not always cause the frequency planner to re-run.

Si5121x Family Changes

Changed maximum input frequency from 166 MHz to 165 MHz

Version 2.8 [2016-4-24]

Add support for Si5342H and Si5344H. These are 2- and 4-output high frequency, ultra-low jitter attenuating clocks with digitally controlled oscillators.

Si538x/4x:

- Fixed: writing a project to the field programmer with a pre- production device would generate an error on 2nd or later writes
- Fixed: the first voltage measurement on an Evaluation Board after power up could be off significantly; this would normally surface as low VDD reading on “Read All”
- Improved support for pre-production devices

Si5121x:

- Update EVB user guide links
- Update pin editor to reflect that SSON input is active low

Version 2.7.1 [2016-4-20]

Add Support for Si5121x Family of Clock Generators:

- Devices: Si51210, Si51211, Si51214, and Si51218
- EVBs: Si51211-EVB and Si51218-EVB

Si538x/4x:

- Fixed: on single DSPLL parts, setting name for 0x0511[5:0] was FAST_BW_PLL instead of FAST_BW3_PLL; this change affects design reports and setting exports
- Fixed: the clock placement wizard could crash if a frequency had never been entered on an output clock
- Adjust calculation of Fastlock Bandwidth coefficients in plans with low Fpfd (near 8kHz) to ensure LOL operates properly when transitioning from Fastlock to phase lock. If affected by this change, when CBPro project file is opened you will be notified of frequency plan change and be prompted to save your updated design to a project file. Changes may occur to Fastlock bandwidth coefficient settings and LOL related DUT settings (registers).
- Added support for 46 ohm LVCMOS impedance @ 1.8V
- Increased 40/41 XO range from 120M to 200M
- Changed Si5340/41 LOS clear threshold default for new designs to 4, so that it passes the design rule check
- Improved XO-related documentation on XA/XB wizard page on Si5342/44/45/80
- Improved support for pre-production devices

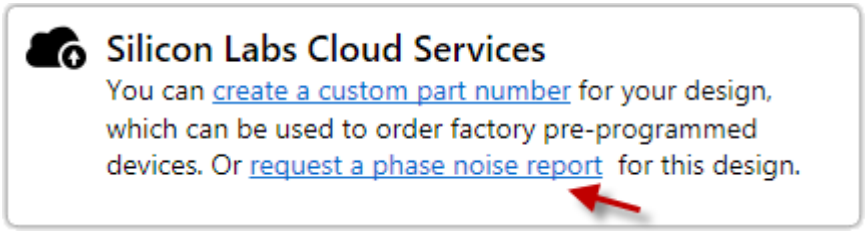
Version 2.6 [2016-3-29]

Bug Fixes:

- Fixed: entering typo or other bad input for clock frequency would crash CBPro
- Fixed: the clock placement wizard did not take into account output names used in frequency expressions. After a manual or automatic reorder, expressions were not adjusted and further editing would lead to unpredictable results.
- Fixed: setting a GPO in the EVB GUI had no effect
- Fixed: frequency plan might not recalculate when an error in design was resolved and the plan was now out-of-date
- Fixed: in the power model to EVB comparison results, the VDD and VDDA measured values were swapped, leading to incorrect difference % listed
- Fixed: TOOL_VERSION decode was wrong in EVB GUI's Info tab
- Fixed: on 41/45 variants, an integer M, fractional P solution might not be used in plan even when possible

New Phase Noise Measurement Service

- Provides a way you can request a custom phase noise report – created by Silicon Labs support engineers in our lab – for one or more outputs in your Si538x/4x design.
- Click the link in the design dashboard Cloud Services section (lower left):



- You will need a www.silabs.com account to make a request.

Si538x/4x:

- Si5346/47/48: stop setting Mx_NUM/Mx_DEN and Nx_NUM/Nx_DEN to 1/1 left shifted when DSPLL is not used; also, stop setting FRACN_CLK_DIS_PLLx to 1 in this case as it is a don't care
- Max output frequency support extended to 712.5M on Si5346/47 rev B
- Max output frequency support reduced to 711.5M on Si5348 rev B. If an output frequency between 711.5M and 712.5M is desired, contact Silicon Labs.
- Small changes to power estimation model
- Improved support for pre-production devices

Misc:

- Export link removed from CBPro home page; open a project file and use the "Export" link on the design dashboard

Version 2.5 [2016-2-23]

DCO:

- Additional detail added to all design reports, including Fout equations and all components used in the equation such as Fvco, Fpfd, and Rx
- Added similar detail to the Si5342H/44H DCO editor
- Fixed instructions clipping issue
- Made setting names in all Fout editor equations match the Family Reference Manual

Automatic Input Clock Switching:

- No longer write input clock priority related settings when manual mode is used.
- Input clock priority no longer has a gap for un-assigned inputs

Misc:

- Fixed: on Si5348/83, LOS_INTR_MSK[3] and OOF_INTR_MSK[3] were always 1 and were not editable in CBPro, causing LOS and OOF on REF to never contribute to INTRb.
- Si5340/41: REFCLK_EN, REFCLK_CLK2PLL_EN, and FRACNP_CLK_DIS are now optimized for case where IN0-IN2 and IN3(ZDB_IN) are not used.
- Improved support for pre-production devices
- Updated description of Si538x/4x Revertive Input Clock Select Mode
- Updated Target Holdover Exit Bandwidth label on DSPLL page
- Updated SPI 3-/4-wire descriptions
- Block Orderable Part Number creation (OPN) on Windows XP: not supported

Version 2.4.0.3 [2016-1-8]

Digitally sign the USB drivers so they can be installed easily on Windows 10. Update CBPro installer digital signature to avoid publisher warnings.

Version 2.4 [2015-12-8]

Misc:

- Fixed: DUT revision check was not being handled correctly with field programmer when writing design/project to volatile memory, giving incorrect error about revision mismatch
- Fixed: on Si5346/47/48, frac(Px) less than 5 could be permitted when non-zero ppm frequency offset workaround was enabled
- Fixed: opening very old project file (CBPro 0.7 and earlier) could crash CBPro
- Updates to EVB GUI “Create DUT Dump” tool (used to send device volatile and non-volatile configuration snapshot to Silicon Labs support personnel)
- Updates for pre-release devices

Si5348:

- Fixed: disabling non-zero ppm frequency offset did not affect MB divider search
- Fixed: Fvco was fixed value optimized for 48MHz XA/XB default, instead of varying based on XA/XB. This could cause non-optimized dividers to be selected when using an XA/XB that is not the 48 MHz default.
- Change Fpfd(max) from 2M to 2.048M; this will raise Fpfd when IN3/4 is above 2 MHz, potentially improving performance.

New Si5346/47 Frequency-On-The-Fly Command Line Tool:

- CBProSi534x8xFOTF.exe is the tool name
- This tool is used to define alternate output frequency plans for a supported device
- Tool output are register write scripts to load base config and switch to a single DSPLL to an alternate plan, plus various reports and support files
- Currently only Si5346/47 multi-PLL devices are supported
- Handles the requirement that Fpfd be fixed across frequency plans when a DSPLL shares an input of another DSPLL
- Type **`CBProSi534x8xFOTF.exe --help`** from a DOS prompt to review the user manual, including an example

- The example described in the user guide can be downloaded from http://www.silabs.com/internal-apps-management/Timing/cbpro/Si538xFOTF-CLI-User-Manual-Example.zip (the link is provided in the user guide)

CBProProjectEdit Command Line Tool Improvements:

- You can now edit DSPLL bandwidth
- Example for single DSPLL device:
  OLBW,,100 Hz
  FLBW,,1k
- Example for multi-DSPLL device:
  OLBW,,A,100
  FLBW,,A,1k
  OLBW,,B,200
  FLBW,,B,2k
- You can also specify bandwidth for multiple DSPLLs at once:
  OLBW,,AB,100 Hz
  FLBW,,AB,1 kHz

Version 2.3.1 [2015-11-4]

Fixed: opening a very old CBPro project file, such as created before version 0.7, could crash the GUI.

Version 2.3 [2015-10-26]

Bug Fixes:

- Fixed: IN3/IN4 on Si5348 could erroneously trigger Px divider Design Rule violations
- Fixed: on 46/47/48, Fdco for PLLs that have the same single unique frequency might be different (for example, 100M,100M on A, 100M on C)
- Fixed: on Si5380, the EVB GUI *Compare Design Estimates to Measurements* tool would report 0 (zero) estimated current/power on VDDO0 and VDDO9 if only the "A" output was enabled (but the estimated total values were correct).
- Fixed: bad pin names on Si5348 output diagram
- Fixed: the Jitter Attenuator Clock Products link on CBPro home page was broken

Si5348:

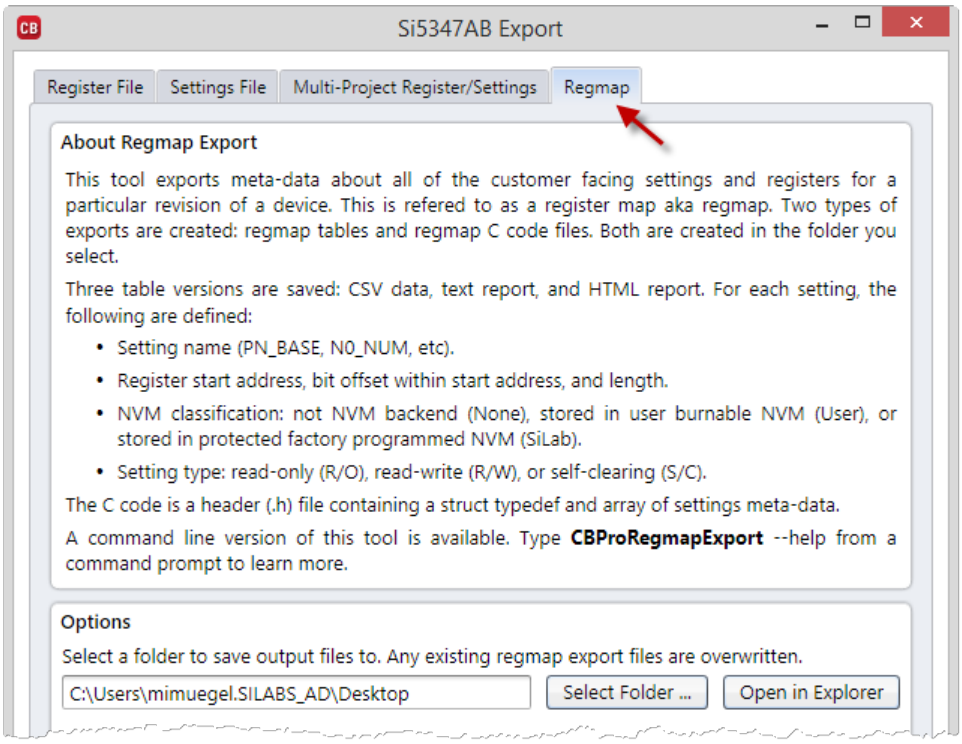
- DSPLL B configuration page is now hidden in the wizard; there is no need to configure DSPLL B
- Default bandwidth settings for new designs and the EVB sample project changed to 100 Hz (open loop and Fastlock).
- New DRC if BW not 100 Hz on DSPLL B.
- Please contact Silicon Labs if your existing design uses a DSPLL B bandwidth that is not 100 Hz.

Misc:

- Fractional Px divider less than 5 will no longer be selected by the frequency planner
- Improvements and support for pre-release devices

Export Improvements & Additions:

- New register map (aka regmap) tab in the GUI's export tool:



- This creates:
  - Regmap tables: CSV, text, and HTML regmap tables for the user's part+revision
  - Regmap as C code: C code definition of the regmap

  Where a regmap contains meta-data about each setting (register bit field) on a device, such as starting address and # bits for a setting

  Example table (HTML shown; CSV and text versions also created):

Setting Name	Location	Start Address	Start Bit	Num Bits	NVM	Type
DIE_REV	0x0000[0:3]	0x0000	0	4	None	R/O
PAGE	0x0001[0:7]	0x0001	0	8	None	R/W
PN_BASE	0x0002[0:15]	0x0002	0	16	SiLab	R/W
GRADE	0x0004[0:7]	0x0004	0	8	SiLab	R/W
...	...	...	...	...	...	...

  Example C header file:

```
#define SI5345_REVB_NUM_SETTINGS                        373
#define SI5345_REVB_MAX_NUM_REGS                        10

#define SLAB_NVMT_NONE 0
#define SLAB_NVMT_SLAB 1
#define SLAB_NVMT_CUST 2

#define CHAR     char
#define UINT8    unsigned char
#define UINT16   unsigned int
```

```
typedef struct
{
        CHAR*  name;            /* Setting/bitfield name                                              */
        UINT8  read_only;       /* 1 for read only setting/regs or 0 for read/write                   */
        UINT8  self_clearing;   /* 1 for self clearing setting/registers or 0 otherwise               */
        UINT8  nvm_type;        /* 0 for not NVM backed; 1 for "silabs" bank; 2 for "user" bank       */
        UINT8  bit_length;      /* Number of bits in setting                                          */
        UINT8  start_bit;       /* Least significant bit of the setting                               */
        UINT8  reg_length;      /* Number of registers that the setting is stored in                  */
        UINT16 addr[SI5345_REVB_MAX_NUM_REGS];   /* Addresses the setting is contained in            */
        UINT8  mask[SI5345_REVB_MAX_NUM_REGS];   /* Bitmask for each register containing the setting */
} si5345_revb_regmap_t;

si5345_revb_regmap_t const si5345_revb_settings[SI5345_REVB_NUM_SETTINGS] =
{

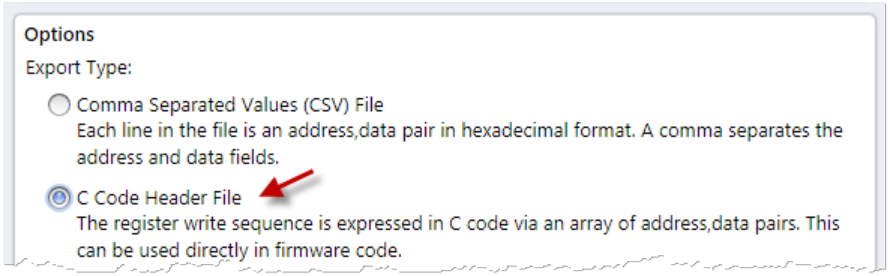
        /* DIE_REV */
        {
                "DIE_REV",
                1, /* 1 = IS Read Only */
                0, /* 0 = NOT Self Clearing */
                SLAB_NVMT_NONE, /* Not stored in NVM */
                4, /* 4 bits in this setting */
                0, /* setting starts at b0 in first register */
                1, /* contained in 1 registers(s) */
                {
                        0x0000, /* Register address 0 b7:0 */

                },
                {
                        0x0F, /* Register mask 0 */

                }
        },
         …
}

/* Setting indexes into si5345_revb_settings array */
#define            SI5345_REVB_DIE_REV 0
#define               SI5345_REVB_PAGE 1
#define            SI5345_REVB_PN_BASE 2
#define              SI5345_REVB_GRADE 3
#define         SI5345_REVB_DEVICE_REV 4
…
```

- New command line tool CBProRegmapExport.exe that does the same thing
- Register File export updated with new C code mode (similar to “Jump Start” option in other Silicon Labs Timing tools):



Example output:

```
#define SI5345_REVB_REG_CONFIG_NUM_REGS                         418

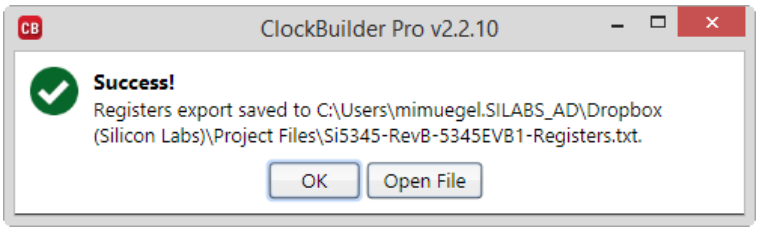
typedef struct
{
        unsigned int address; /* 16-bit register address */
        unsigned char value; /* 8-bit register data */

} si5345_revb_register_t;
```

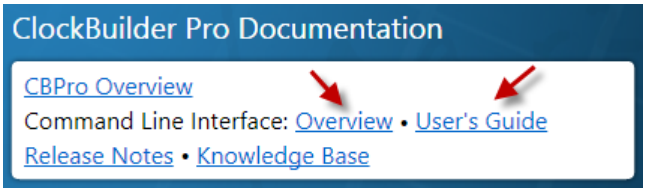
```
si5345_revb_register_t const si5345_revb_registers[SI5345_REVB_REG_CONFIG_NUM_REGS] =
{
        { 0x000B, 0x68 },
        { 0x0016, 0x02 },
        { 0x0017, 0x1C },
        { 0x0018, 0x00 },

        …
}
```

- Existing CBProProjectRegistersExport.exe CLI updated to support exporting existing CSV format or new C code format. You now must specify the type of output via `--format csv` or `--format cheader`
- GUI export now shows confirmation dialog in all cases, which button to open file/folder:



- The Command Line Interface (CLI) overview and user's guide has been updated. This is available from the home screen of CBPro:



Version 2.2 [2015-09-10]

Design Rule Updates:

- Removed warning if fastlock bandwidth is less than 10x open loop bandwidth.
- Added new warning if LVCMOS impedance selected is not the lowest available value:

Warning	OUT0: For the best signal integrity, Silicon Labs strongly recommends selecting the lowest LVCMOS output impedance (24 Ω) and then choosing the proper external source resistor to produce the best signal shape at the end of the signal trace

Misc:

- Exclude PXAXB, P0_FRACN_EN, and FRACNB_EN from Si5380 exports and design reports: these settings have fixed values. The default DUT values are never modified by CBPro.
- Work around for lack of field programmer wire/socket mode selector on the design dashboard: the field programmer is forced to "wire" mode (field programmer connected to system board via SPI/I2C serial connection) in this case. A mode selector will be added to the dashboard in a future release of CBPro.

Bug Fixes:

- Fixed: when outputs were manually assigned to an N divider, in rare cases CBPro could not find a plan solution when it should be able to.
- Fixed: when Zero Delay Mode was enabled, you could get an invalid warning about input-to-output phase delay with certain frequency plans.

- Fixed: the Named Systems Monitor menu item was missing in CBPro 2.1; this is available when you have created or opened a project file, and allows you to monitor changes to proposed DUT settings as you change your design goals.

Version 2.1 [2015-08-18]

New Devices:

- Support added for Si5347CD, a 4-Output Quad DSPLL Any-Frequency Jitter Attenuating Clock Multiplier.
- Support added for Si5348, a 7-Output SyncE/IEEE-1588 Telecom Boundary Clock Synchronizer. Contact Silicon Labs for access.

New DCO Support:

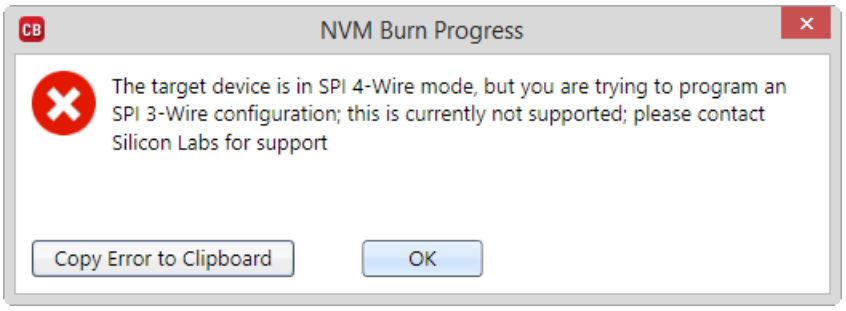
- Digitally-Controlled Oscillator (DCO) mode can be used by to make small, glitchless frequency changes on supported Si538x/4x devices. Changes are made by host via I2C/SPI or pin control (where supported).
- Available on Si5340/41/42/44/45/46/47/48.
- The DCO editor is a new page in the CBPro Wizard, immediately after the output frequency page.
- An **introductory video** is available (and is linked to from the CBPro DCO page).
- Refer to your device's Family Reference Manual for detailed information on DCO mode.

ClockBuilder Pro Field Programmer:

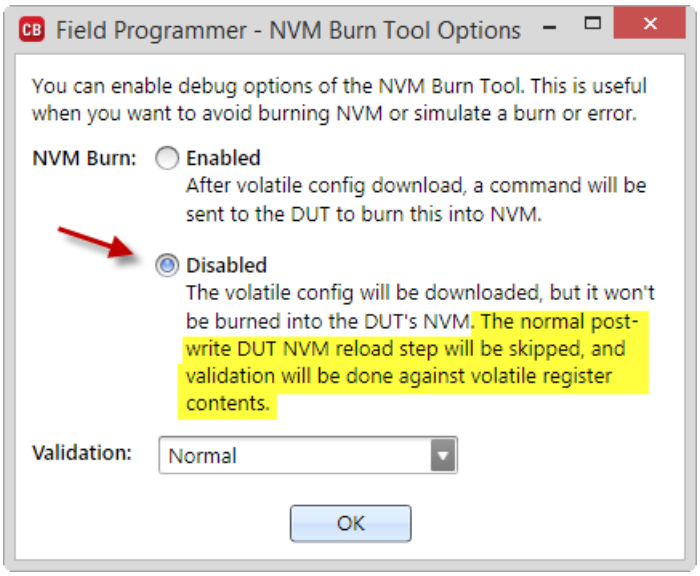
- Loosened requirements for "baseline" NVM state on programming target for Si538x/4x revision "B". If baseline 22 device is present, you will no longer receive the following warning:



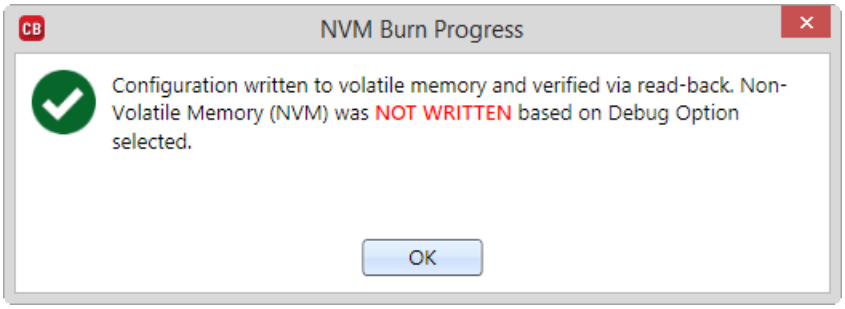
- Socket-based burns are currently limited to SPI 4-wire mode. If you are trying to burn a project file that configures 3-wire mode, the burn will be cancelled with the following notice:



- Changed the behavior of the field tool debug options. NVM Burn->Disabled now skips the NVM reload step, ensuring that the DUT is left with the new config in volatile memory and the validation should normally pass



And the confirmation dialog explains this:



Misc:

- The Clock Placement Wizard has been improved to better isolate outputs capable of contributing to jitter.
- Design Rule Check (DRC) improvements.

Bug Fixes:

- Fixed: on Si5340/41, if XA/XB is mixed with standard INx clock inputs and a fractional M divider was required, the frequency planner could not find a solution.
- Fixed: on Si5346/47, N_PIBYP register setting is no longer actively set based on frequency plan. It will always be set to 0.
- Fixed: if “optimize plan for zero ppm frequency offset” was unchecked on Si5346/47 and hitless switching was turned off, Fdco could be higher than necessary.
- Fixed: the “optimize plan for zero ppm frequency offset” checkbox was shown on the Si5340/41 output editor page in the Wizard, even though it had no effect on frequency plan and did not apply to these devices.
- Fixed: in very rare circumstances, trying to open a project file can yield “cannot access a closed file” error
- Fixed: in CBProProjectEdit command line tool, if the edit file results in an unrealizable plan, you could get a message “Object reference not set to an instance of an object” instead of planner error details.

Version 2.0.2 [2015-06-16]

Bug Fixes:

- Fixed: if a frequency plan could not be calculated, clicking the design report could crash CBPro.
- Fixed: an ultra-low frequency input such as 8 kHz, with unrelated outputs, could result in no frequency plan on Si5340/41/42/44/45.
- Fixed: the Si5380 EVB User's Guide PDF shortcut was not valid.
- Fixed: on PCs with "large fonts" (high DPI) enabled, edit page shortcuts in the dashboard could be clipped.

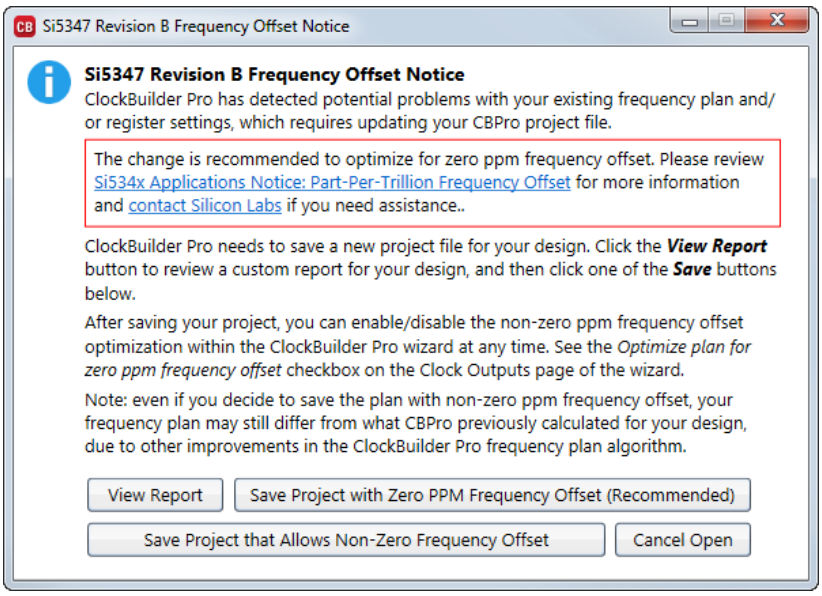
Version 2.0 [2015-06-15]

Misc:

- The Si5380 ultra-low phase noise jitter-attenuating clock generator can now be selected in CBPro. You can create a new design, or open a sample design that matches the Si5380 Evaluation Board configuration.
- Zero Delay Mode (ZDM) is now fully supported on Si5340/41/42/44/45/80. ZDM is available for applications that require fixed and consistent minimum delay between the input clock and outputs.
- Output Skew (aka Phase Delay) is now supported on Si5340/41/42/44/45/80. This feature is available for applications that need a specific output skew configuration. This is useful for PCB trace length mismatch compensation.
- The frequency planner now favors integer M (Si5340/41/42/45/80) and integer MA-BD (Si5346/47), as long as it can do so with Fpfd 1 MHz or higher. This may improve jitter performance for certain designs.
- Default Fastlock bandwidth changed to 1 kHz (10x nominal 100 Hz default)
- Sample designs (plans) have been updated for Si5342/44/46/80.

Part-Per-Trillion Frequency Offset:

- A frequency offset issue in a small percentage of Si534x devices' frequency plans can result in an offset between <1 and 10,000 parts-per-trillion (ppt). This frequency offset issue can affect any of the following: Si5342/44/45/46/47.
- CBPro has been updated to address this issue via an enhanced frequency planner algorithm. If you open your existing project file in CBPro 1.9 or higher, it will be inspected to determine if it has the issue. If your existing design has the issue, you will receive this notice:

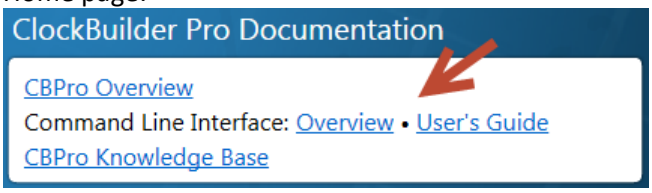


If you do not see this notice, your existing design is not effected by the issue.

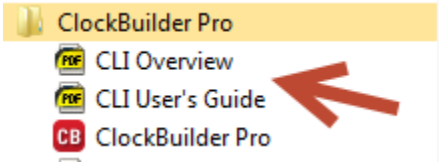
- Please read Si534x Applications Notice: Part-Per-Trillion Frequency Offset for more information.

Command Line Interface (CLI):

- The CLI allows you to perform batch oriented project edit, frequency planning, and export activities from the command line. Note the CLI tools have always been bundled with CBPro, available in C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\Bin.
- New in this release: CLI documentation and samples are now bundled with CBPro.
- Documentation:
    - Home page:



    - Start Menu:



- The CLI samples -- project files, edit files, and DOS batch files – are in C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\CLI. The User's Guide references these.

Version 1.8 [2015-04-30]

Support added for the new ClockBuilder Pro Field Programmer Kit. This kit allows you to program a Si538x/4x device "in-system" using I2C or SPI. Volatile and non-volatile programming modes are supported. Socket-based programming can also be performed, including burning a CBPro project file to NVM on a loose device. Please read the ClockBuilder Pro Field Programmer Kit User Guide to learn more.

Your target nominal loop bandwidth can be achieved in more cases. Previously, 2 kHz and 4 kHz selections could never be achieved.

If nominal loop bandwidth would result in increased output jitter and/or increase peaking, a new DRC warning will be displayed and added to your design report.

Si5380 LVDS amplitude register settings updated for 1.47456 GHz output.

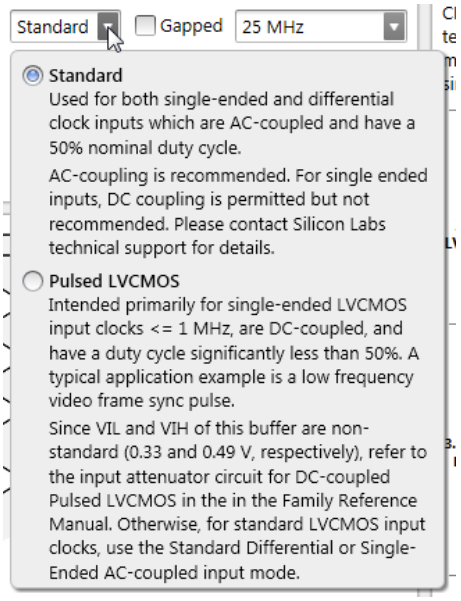
Version 1.7.1 [2015-04-03]

Fixed: the EVB GUI would not launch when connected to the Field Programmer dongle.

Version 1.7 [2015-03-26]

Input Buffer Changes:

- Previous differential selection now labeled Standard. Previous CMOS selection is now labeled Pulsed LVCMOS, with updated explanation for each:



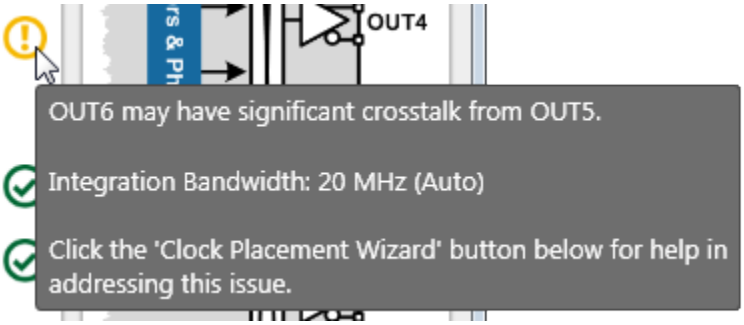
- The CMOS option has been removed outright from the Si5340/41 wizard, as the CMOS selection has not been used for these devices and had no effect.
- New Pulsed LVCMOS diagram.
- If Pulsed LVCMOS is selected, a Design Rule Check (DRC) warning will be generated.
- The IN_CMOS_EN DUT setting has been renamed IN_PULSED_CMOS_EN.

New Output Crosstalk-Related Features:

- On the output frequency page of the wizard, potential crosstalk issues are now flagged and shown directly in the editor:



- Move your cursor over the icon to learn more:

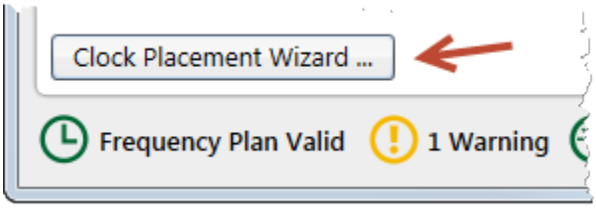


- There are three possible icons that can be shown:
  - No crosstalk issues expected.
  - Potential fundamental (1st order) crosstalk issues.
  - Potential 2nd, 3rd, or 4th order crosstalk issues. The icon will get dimmer from 2nd to 4th order.

- A DRC will continue to be generated:

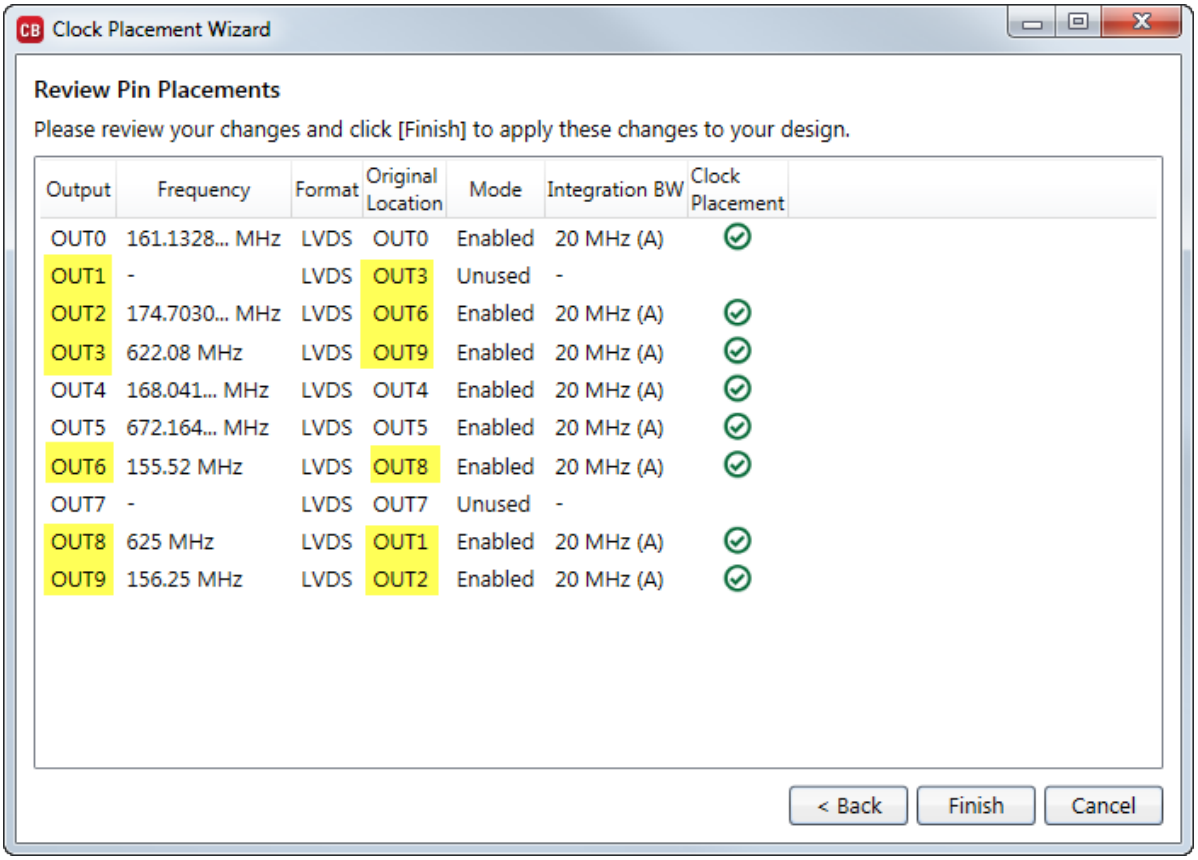
  1 Warning

- A new Clock Placement Wizard is available that will optimize output clock pin placement to minimize jitter and potential crosstalk issues. Click the new “Clock Placement Wizard” button that is located at the bottom left of the output frequency page:



- The clock placement wizard supports a fully automatic mode as well as a manual mode, where you can reposition output frequencies via drag-and-drop.

- Example of automatic mode placement. Before and after columns indicate which frequencies were moved:

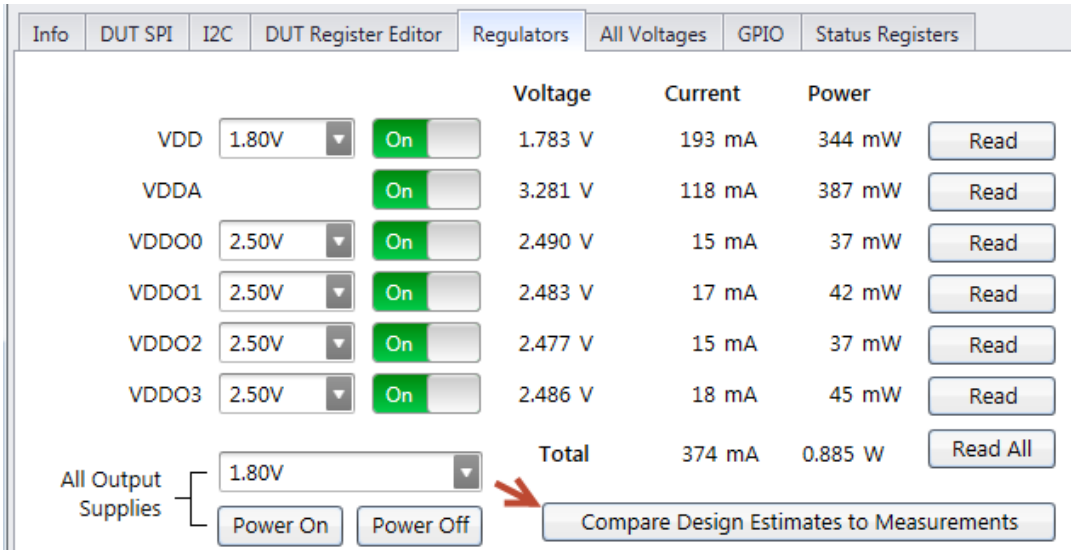


Output	Frequency	Format	Original Location	Mode	Integration BW	Clock Placement
OUT0	161.1328... MHz	LVDS	OUT0	Enabled	20 MHz (A)	✓
OUT1	-	LVDS	OUT3	Unused	-	
OUT2	174.7030... MHz	LVDS	OUT6	Enabled	20 MHz (A)	✓
OUT3	622.08 MHz	LVDS	OUT9	Enabled	20 MHz (A)	✓
OUT4	168.041... MHz	LVDS	OUT4	Enabled	20 MHz (A)	✓
OUT5	672.164... MHz	LVDS	OUT5	Enabled	20 MHz (A)	✓
OUT6	155.52 MHz	LVDS	OUT8	Enabled	20 MHz (A)	✓
OUT7	-	LVDS	OUT7	Unused	-	
OUT8	625 MHz	LVDS	OUT1	Enabled	20 MHz (A)	✓
OUT9	156.25 MHz	LVDS	OUT2	Enabled	20 MHz (A)	✓

New Estimated vs. Measured Current/Power Comparison Tool:

- In the EVB GUI, you can now compare actual current/power as measured on the EVB using the built-in EVB sensors vs. what CBPro estimated and shows in the power widget / design report.

- Click this button:



- Example report:

Assumptions

VDD: 1.8 V **Ta:** 70 °C **Airflow:** None

	Frequency	Format	Estimated			Measured			Power Delta
			Voltage	Current	Power	Voltage	Current	Power	
VDD	N/A	N/A	1.8 V	192.6 mA	346.8 mW	1.782 V	194.0 mA	345.7 mW	-0.3 %
VDDA	N/A	N/A	3.3 V	116.4 mA	384.0 mW	3.276 V	116.0 mA	380.0 mW	-1.0 %
VDDO0	161.132812... MHz	LVDS	2.5 V	16.0 mA	39.9 mW	2.490 V	15.0 mA	37.4 mW	-6.5 %
VDDO1	644.53125 MHz	LVDS	2.5 V	19.2 mA	48.0 mW	2.488 V	17.0 mA	42.3 mW	-11.9 %
VDDO2	174.703083... MHz	LVDS	2.5 V	16.1 mA	40.2 mW	2.478 V	14.0 mA	34.7 mW	-13.6 %
VDDO3	698.812334... MHz	LVDS	2.5 V	19.6 mA	48.9 mW	2.487 V	18.0 mA	44.8 mW	-8.4 %
			Total	380 mA	908 mW		374 mA	885 mW	-2.5 %

Misc:

- OUTx_CM common mode setting for LVDS at 1.8V VDDO changed from 14 to 13.
- Stop-mid disabled state is now longer available.
- Improved support for pre-release devices.

Version 1.6.1 [2015-02-12]

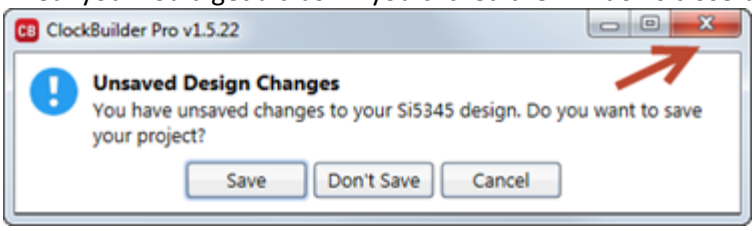
Fixed: prepare orderable part number wizard for Si538x/4x revision B.

Version 1.6 [2015-02-11]

Bug Fixes:

- Fixed: 46/47: don't run DRC on DSPLLs that have not been assigned to an input.
- Fixed: if you changed power/Tj estimation assumptions and quit CBPro, future launches of CBPro would give a fatal error because the CBPro process was still active in the background.

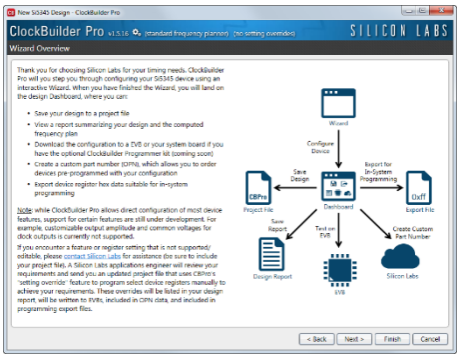
- Fixed: DRCs related to frac P/gapped clock/BW restrictions triggered false error for certain mixed input scenarios.
- Fixed: power widget was not showing warn/error icon when XTAL-based Tj limits were reached
- Fixed: on Si5380, the customer register names related to OUT0, OUT0A, and OUT9A were incorrect. Thus design reports, datasheet addendums, and setting exports were incorrect.
- Fixed: you would get a crash if you clicked the Windows close button on the unsaved changes dialog:



Now clicking will be the same as cancel.

Misc:

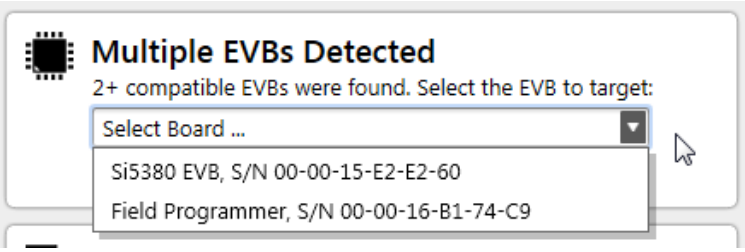
- A new CBPro introduction page is displayed in the wizard when you create a new design:



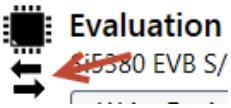
- Includes Beta support for upcoming ClockBuilder Pro Field Programmer device. This kit will allow customers to write their configuration to a Si538x/4x device located on a system board via I2C or SPI. The kit also supports burning NVM of a DUT on either a system board or included kit socket board.

Improved Multiple EVB Support

- When you open a project and there are 2+ combined of EVB(s) that are compatible or field programmer(s), CBPro now provides an option to select which one to target:



- Once selected, you can switch to targeting another board via the two arrows icon:



Si538x/4x:

- Supports creating Si5340/41/42/44/45/46/47/80 Revision B Custom Part Numbers (OPNs) after PCN is published.
- Revision B is now assumed when you are editing a design. This only factors into the junction temperature (Tj) limits used in the power/Tj estimation calculations.

- Si5346/47: frequency planner algorithm optimizes for low output jitter by adjusting Fdco/R dividers.
- Si5340/41: the setting name for the 0x0018[0:3] register has been changed from LOSFB_IN_INTR_MSK to LOSIN_INTR_MSK to be consistent with related registers LOSIN and LOSIN_FLG.
- Si5380: AMPL and CM driver settings now vary for 1.2288 GHz and 1.47456 GHz output frequencies in LVDS and LVPECL modes.
- Any Tj warning or violation that would be displayed in the power widget and power section of the design report will now generate an equivalent Design Rule Check (DRC) warning.
- The EVB GUI now shows HOLD_HIST_VALID and FASTLOCK_STATUS status bits in the Status tab.
- For devices with fixed grading such as Si5380, the datasheet addendum now lists that grade instead of "X" placeholder. For example:

  Si5380A Datasheet Addendum
  Device Configuration Summary for Si5380A-XXXXXX-GM

- 40/41: in design report, XA/XB moved into Inputs section and always shown, even if not used:

```
Inputs:
   XAXB: Unused
    IN0: 48 MHz
         Differential
    IN1: 48 MHz
         Differential
    IN2: Unused
```

```
Inputs:
   XAXB: 48 MHz
         External Reference Clock Mode
    IN0: Unused
    IN1: Unused
    IN2: Unused
```

- The "I am targeting pre-production samples" export option has been removed. This was used to include additional internal registers in exports to "patch" Si538x/4x pre-production samples to current device register baseline. If you are still targeting pre-production samples, please contact Silicon Labs for support.

New Command Line Tools

There are three new command line tools in CBPro, oriented at project edit and export:

CBProProjectEdit	Accepts a project file and a simple text file describing changes to input and/or output clocks in the design. Saves updated design back to a project file.
CBProProjectRegistersExport	A command line version of CBPro's register export tool. Accepts a single project file and creates a register export file.
CBProProjectSettingsExport	A command line version of CBPro's setting export tool. Accepts a single project file and creates a named settings export file.

These join the previously existing multi-project export tool:

CBProMultiProjectExport	A command line version of CBPro's multi-project export tool. This accepts 2+ project files, and outputs unified settings and register export files that define what setting/register differs between each project, and the values for each input project.

Documentation on each tool can be displayed by typing Tool --help at a command/shell prompt. For example:

```
> CBProProjectEdit --help
```

Version 1.5 [2014-12-03]

Loop Bandwidth:

- Fixed: the BW4_PLL/ BW5_PLL DSPLL loop bandwidth coefficient register values calculated by CBPro were incorrect by a factor of two in most cases in CBPro versions 1.3 and 1.4. This would result in actual measured BW ~2x CBPro estimate. This only applies to Si5342/44/45/46/47/80.

- Coefficients are now shown in design report, and included in “plan updated” messages that are shown when you open a project file. This will ensure you are notified of the above bugfix when opening a project file created with an affected version of CBPro.

Frequency Planner:

- On Si5341/45/80, for cases where there was only 1 distinct frequency on an N divider, the N&R dividers are now optimized to favor integer N, low OID tone, and low R in the case of a tie. This will result in lower power consumption and reduced jitter in certain plans having only one unique frequency on an N divider.

OOF (Out-Of-Frequency):

- Fixed: OOF_DIV_CLK_DIS[INx] was being set if precision OOF and fast OOF was disabled on INx. This would erroneously disable OOF functionality. Now CBPro will ensure OOF_DIV_CLK_DIS[INx] is not set if INx is the OOF reference clock.
- If OOF is completely disabled by unchecking all precision and fast OOF checkboxes, the OOF Reference Clock selector is disabled as it will be a don’t care. OOF_DIV_CLK_DIS will be set to 15d in this case.

Misc:

- Timestamps in datasheet addendums, design reports, and exports now show timezone and use a more consistent, culture neutral formatting scheme. For example, from a datasheet addendum:

```
Overview
========
Part:          Si5345
Design ID:     5345EVB2
Created By:    ClockBuilder Pro v1.4.2 [2014-12-02]
Timestamp:     2014-12-02 08:15:44 GMT-06:00
```

Version 1.4 [2014-11-5]

Frequency Planner:

- Updated the Si5342/44/45 frequency planner algorithm to optimize output jitter and minimize output phase transients during a input clock switch (via hitless switching) in certain plans. In previous versions of CBPro, integer Px divider and integer M divider solutions have been favored, regardless of low Fpfd frequency that might result. In this release, integer Px solution with highest Fpfd is favored, even if that selects a fractional M divider.
- Bug Fix: in v1.3, if all outputs were manually assigned to an N divider – i.e. there were no auto N assigned outputs – the planner would fail and you would see a DRC error “sequence contains no elements.”
- Bug Fix: in v1.3, any Fvco_Max frequency planner override defined by Silicon Labs would have been ignored.

Version 1.3 [2014-11-2]

Release Summary:

- As with any new CBPro release, Silicon Labs recommends using the latest version of the software so your designs can enjoy the benefits of the numerous performance, functionality and embedded DRC (Design Rule Check) enhancements of the new software.
- Loop bandwidth-related improvements: CBPro is more likely to achieve your desired nominal and fastlock bandwidth; mid-band phase noise performance has also been enhanced
- LOL improvements: set and clear thresholds are selected for you in “auto” mode make it easier to support a noisy input clock; new relaxed LOL mode; fix for clear timer disable bug
- Frequency planner improvements: much improved phase-frequency detector frequency (Fpfd) selection for certain plans; one fewer N divider used in certain plans, reducing power consumption; lower Fvco frequency selected in certain plans; reduced low-level spurs in certain plans

- New manual N divider assignment feature to support certain advanced in-system plan updates
- Stop mid disabled state is no longer recommended for differential drivers, as recovery is not glitch-less.
- The number of embedded DRCs has been expanded.

Bandwidth Changes:

- Bug Fix: Fastlock bandwidth was being limited based on estimated nominal bandwidth. This would result in much lower Fastlock bandwidth than desired in certain plans.
- The algorithm used to define loop bandwidth coefficients -- BW[0-5]_PLL / BW[0-5]_PLL[A-D], FAST_BW[0-5]_PLL / FAST_BW[0-5]_PLL[A-D], and LOL_CLR_DELAY / LOL_CLR_DELAY_PLL[A-D] -- has been improved. For certain frequency plans, these changes may improve phase noise in the 100 Hz – 1 kHz band.
- The equations used to limit actual maximum loop bandwidth based on your target BW have been improved. Maximum bandwidth is now optimized based on P/M divider state Fvco, Fpfd, Fdco, gapped clock setting, and/or min (Fin). The optimized maximum bandwidth produces the lowest jitter for an integration bandwidth from 12 kHz to 20 MHz.
- Fastlock minimum values that can be selected are now filtered based on nominal selection: fastlock BW cannot be less than nominal BW. A DRC error will be shown if a project file created with previous version of CBPro that allowed this combination.
- New design rule checker warning if fastlock BW is > 100x nominal BW:

Warning	DSPLL fastlock bandwidth should normally be 100x or less than nominal bandwidth. A fastlock loop bandwidth that is greater than 100 times the nominal loop bandwidth value will lock faster. However, it may also introduce transients in the frequency vs. time behavior. For loop bandwidth values of near 0.1 Hz, this tradeoff might make sense. Normally, it should be avoided.

- While ZDB is not fully supported by CBPro with this release, certain Fpfd/BW combinations will result in degraded ZDB performance. These will get flagged as a design rule checker warning:

Warning	ZDB 100ps ip/ip delay cannot be met due to: Fpfd less than 64 kHz

- The minimum input frequency when there is a P divider or gapped input clock is now dynamic based on your approximate nominal BW. This may result in a DRC error condition for certain plans:

Error	Because IN0 is a gapped clock, IN0 must be at least 20.5 MHz for your frequency plan

Please contact Silicon Labs for support if you encounter this condition on existing designs.

Frequency Planner Changes:

- The Si5342/44/45 planner now supports fractional P, fractional M plans. In cases were one of the Px or M dividers do not have the required resolution, a planner error will be shown:

Error	no solution possible due to highly fractional clocks; inspect clock frequency definitions to ensure they are fractional expressions when appropriate (M,P0,P1 divider(s) not realizable)

- The planner reduces low-level spurs on Si5340/41/42/44/45 devices. This may cause formerly integer divider to become fractional to avoid certain Nx divider spur conditions.
- On Si5340/41/42/44/45, the algorithm used to determine what Fvco frequency to use in cases where there are multiple output even common multiple groupings that would yield the same # N dividers has been adjusted. For some plans, a higher Fvco and sometimes fewer N dividers will now be selected, as prioritization is now given to higher N divider Fid in these “tie” cases.

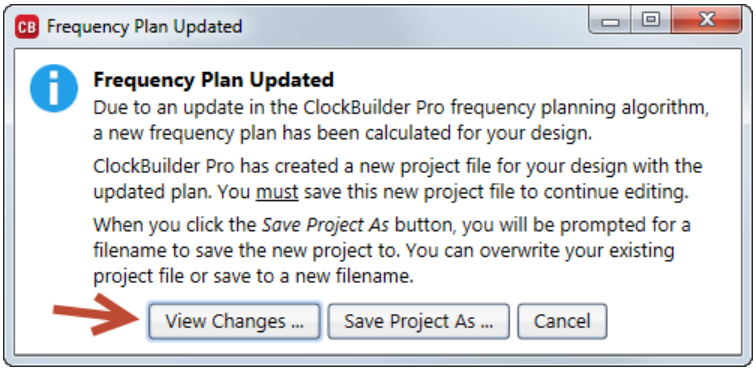
  Example:

  CBPro 1.2 *CBPro 1.3*

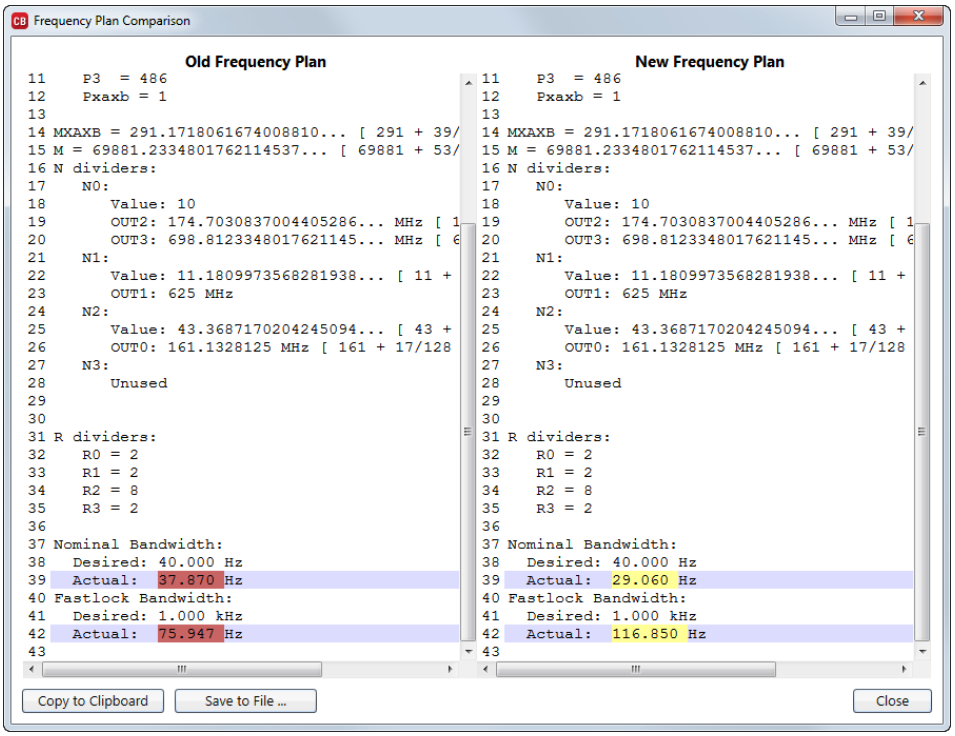
Fvco = 13.5 GHz
N0:
Value: 27
OUT2: 50 MHz
OUT3: 125 MHz
N1:
Value: 10.3846153846153846... [10 + 5/13]
OUT0: 26 MHz
N2:
Value: 250
OUT1: 27 MHz

Fvco = 14.04 GHz
N0:
Value: 10
OUT0: 26 MHz
OUT1: 27 MHz
OUT2: 14.04 MHz [14 + 1/25 MHz]
N1:
Value: 56.16 [56 + 4/25]
OUT3: 125 MHz

- Fixed: On Si5342/44/45/80, the Fpfd frequency selected when finding an integer P, integer M solution (always true for 80) would not select optimal (highest possible Fpfd) M divider in most cases.
- The frequency planner version has been up-revisioned, so opening any existing project will cause the frequency planner and bandwidth coefficient calculator to re-run. If CBPro calculates a new frequency plan for your design – dividers and/or bandwidth coefficients – you will be notified and prompted to save your design to a new project file (we recommend keeping the old file for backup):



New in CBPro 1.3 is the ability to view the differences between old and new project plan using the "View Changes" button. Clicking this will bring up a diff of old and new plan, such as:

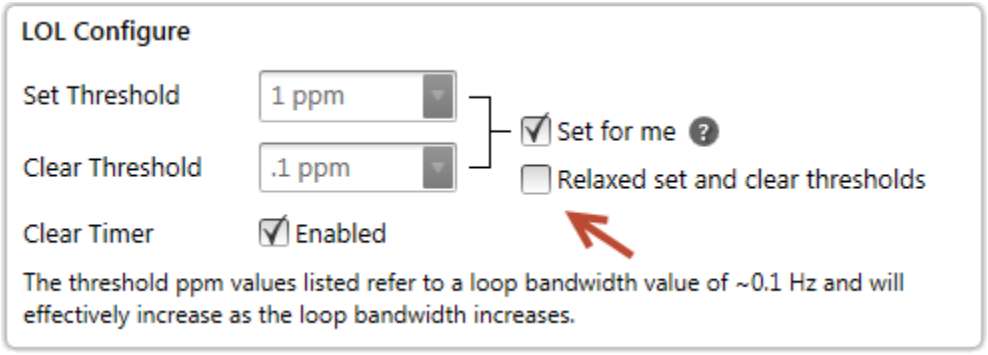


LOL (Loss of Lock) Improvements:

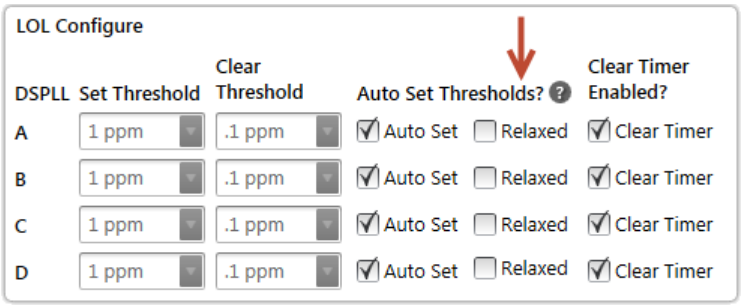
- Fixed: The LOL (Loss of Lock) "Clear Timer Enable" checkbox did not affect the correct DUT setting. Instead of affecting the state of LOL_TIMER_EN / LOL_TIMER_EN_PLL[A-D], LOL_SLOW_EN_PLL / LOL_SLOW_EN_PLL[A-D] was inadvertently being set. This bug would have only been triggered if you tried to disable the clear timer, which is not the default. If you had unchecked "Clear Timer Enable", LOL would have been disabled due to this bug.
- Improved LOL_SLW_DETWIN_SEL and LOL_SLW_VALWIN_SEL settings are defined by CBPro. The changes should make it easier to support a noisy input clock: higher priority is given to a longer detection window size than number of windows. Note DETWIN and VALWIN are never directly set by you in the CBPro wizard: they are set based on plan, bandwidth, and clear threshold.
- The LOL auto set threshold option – which is on by default – now has a new mode to relax the set and clear thresholds.
    - Example of use:

	Normal	Relaxed
Set	30 ppm	100 ppm
Clear	3 ppm	10 ppm

    - Setting on Si5342/44/45/80:



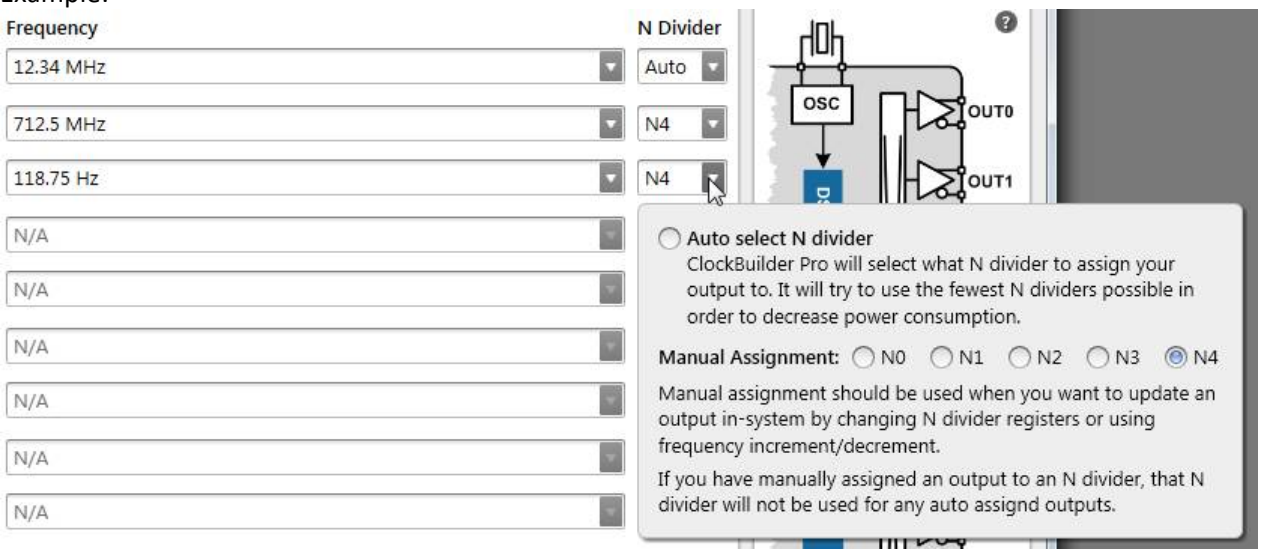
    - Setting on Si5346/47:



New Manual N Divider Assignment Feature:

- A new column has been added to the output frequency page to (optionally) force one or more outputs to a certain N divider. This is useful when you will be doing in-system frequency plan updates and need to ensure one or more outputs are consistently assigned to a certain N divider.
- When a divider is manually selected, that divider will no longer be used for automatic N divider assignment
- This only applies to Si5340/41/42/44/45.
- Divider assignment does not have to be contiguous
- Note: while files created with this version of CBPro can be opened by an earlier GUI, the manual assignments will be ignored and the planner will auto assign those outputs.

- Example:




```
N dividers:
   N0:
      Value: 577.3905996758508914... [ 577 + 241/617 ]
      OUT0: 12.34 MHz [ 12 + 17/50 MHz ]
   N1:
      Unused
   N2:
      Unused
   N3:
      Unused
   N4:
      Value: 10
      OUT1: 712.5 MHz [ 712 + 1/2 MHz ]
      OUT2: 118.75 Hz [ 118 + 3/4 Hz ]

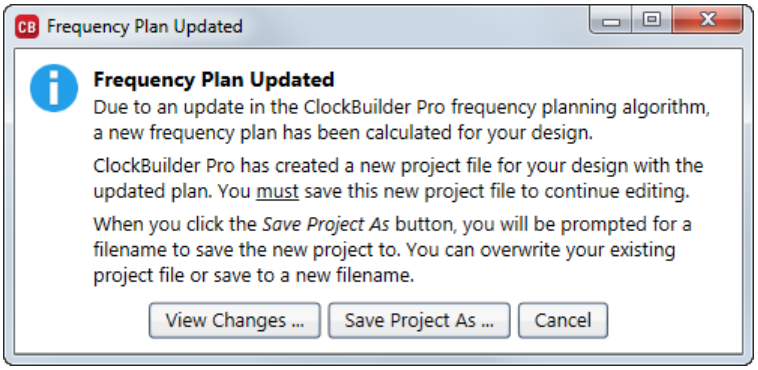
R dividers:
   R0 = 2
   R1 = 2
   R2 = 12000000
```

- If the outputs manually assigned to a divider are not even common multiples, a DRC error will be triggered:
  Some of your manual N divider assignments are not valid because there are no common even multiples between all output frequencies across the N divider output range:
  - - N4: OUT1,OUT2,OUT3

EVB GUI:

- The EVB GUI now fully supports the Si5342 evaluation board.
- The Si5340 EVB and Si5341 EVB default plans have been updated: IN0-IN2 are no longer enabled, which will ensure LOS does not cause INTRb to be asserted.

- The Write Project File feature now checks to see if the frequency plan was saved with older version of planner. If it was, a new plan is calculated. If the new plan differs from old, the same plan change dialog is shown to the user that the Wizard project open would show:



  In order to write the project, it must be saved. So now the EVB GUI experience when working with out-of-date plans is in sync with Wizard.
  Note that previously, the plan would be automatically recalculated behind the scenes, so you always got the new plan (which you might not realize).

Misc:

- The 0x0B44[5] setting name on Si5342 was changed from MDIV_FRANC_DIS to FRACN_CLK_DIS_PLL.
- Added DRC warning when CMOS buffer mode is used on Si5340/41:

Warning	Using the CMOS input buffer option may result in jitter higher than when differential input buffer mode is selected. Silicon Labs strongly recommends using the differential input buffer option with the LVCMOS input termination circuit shown in the Si5341/40 Reference Manual.

- On Si5342/44/45, always set PLL_OUT_RATE_SEL to 1 to ensure expected behavior when using XO in range 30 MHz – 44 MHz.
- Stop-mid disable state is no longer recommended because recovery is not glitch-less. The sample projects and EVB sample plans bundled with CBPro have been changed to stop low disabled state. If your existing design uses stop mid, a design rule warning will be generated.

Version 1.2 [2014-09-09]

Bug Fixes:

- Fixed: 40/41/42/44/45 frequency planner could select invalid N (below 10) in certain edge cases.
- Fixed: the GUI could crash when entering output frequencies under certain rare conditions.
- Fixed: a crash could result if the software updater found a new version in the background, you had closed CBPro wizard, and EVB GUI was not active.

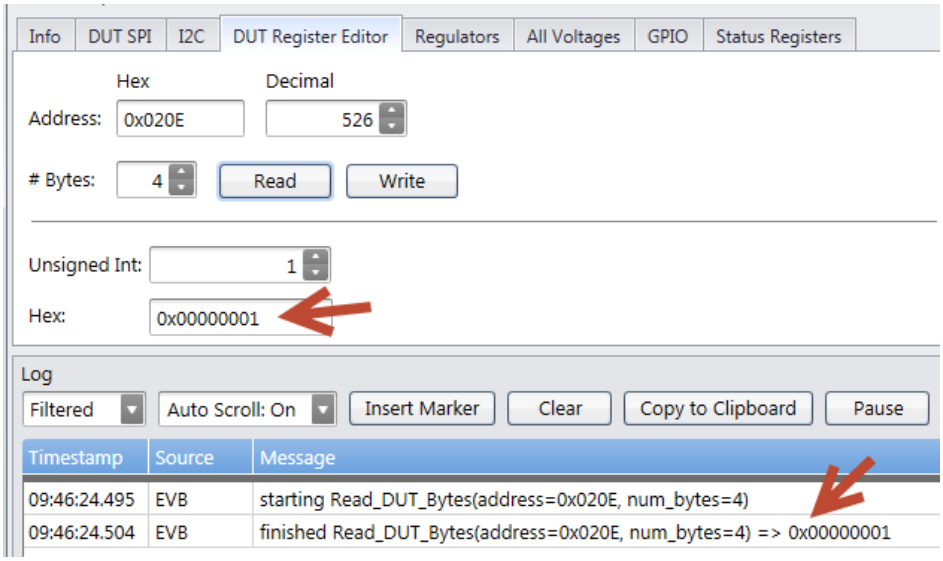
Write Design to EVB:

- Changed order in which output regulators are turned on and synced to I/O voltage defined in project file
- Old:
  - Enable VDD/VDDA
  - Write registers including soft reset/etc
  - Enable/set level of VDDOx
- New:
  - Enable VDD/VDDA
  - Enable/set level of VDDOx
  - Write registers including soft reset/etc

- This ensures all output buffers will be property initialized to the same phase when the device soft reset completes.

EVB GUI:

- Changed byte ordering in register editor results/editor and logging:



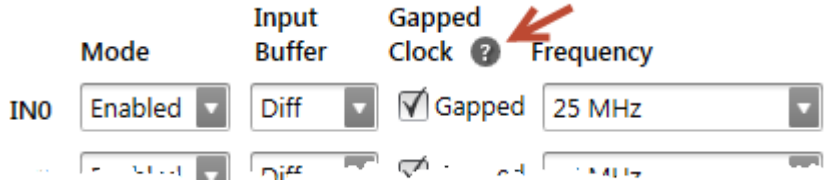
Version 1.1 [2014-08-13]

Bug Fixes:

- Fixed: in register exports when “I am targeting pre-production samples” was checked, register 0x0A06=0 containing device trim data was being included in the export. Writing this register to your pre-production samples could reduce performance.

Loss of Lock (LOL) Improvements:

- The LOL set/clear threshold values that are calculated for you when you select “set for me” on the LOL page are now defined based on the state of Px (integer vs fractional), gapped clock checkbox (see below), Mx outer loop state (integer vs fractional), and input frequencies or Fdco. Affected device settings are LOL_SLW_SET_THR, LOL_SLW_CLR_THR (42/44/45) and LOL_SLW_SET_THR_PLLx, LOL_SLW_CLR_THR_PLLx (46/47).
- Computation of LOL_SLW_DETWIN_SEL, LOL_SLW_VALWIN_SEL, LOL_CLR_DELAY (42/44/45) and LOL_SLW_DETWIN_SEL_PLLx, LOL_SLW_VALWIN_SEL_PLLx, LOL_CLR_DELAY_PLLx (46/47) has also been updated. The values selected are now based on bandwidth coefficients and plan VCO frequency.
- These new default values and register settings yield faster lock times when using fast lock, and less likelihood of false positive and false negative LOL status conditions.
- You can now mark an input clock as being gapped. This will influence LOL set/clear threshold “set for me” values:



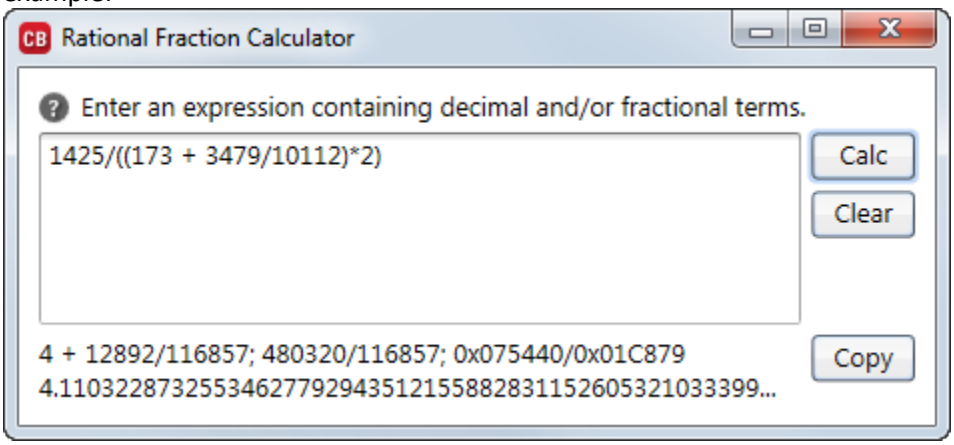
- The LOL threshold table was not in sync with actual device values:
    - Old: 0.2 ppm, 0.6, 2, 6, 20, …
    - New: 0.1 ppm, 0.3, 1, 3, 10, …
- To handle existing projects, if CBPro detects an invalid (i.e. old) PPM value, it will switch the DSPLL to “set for me mode”, which is the default for new designs.

Misc:

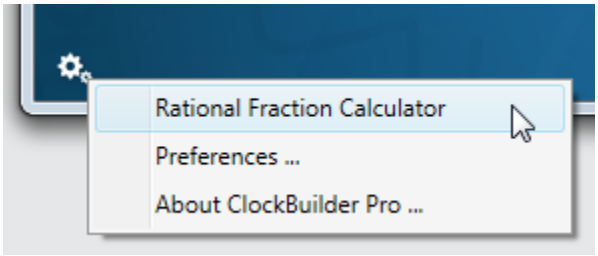
- NVM controller configuration register (0x1002=7) and settings (SLAB_NVMC_SILABSECCCHK_EN=1 and SLAB_NVMC_USRECCCHK_EN=1) were being included in exports when “I am targeting pre-production samples” was checked. These are no longer patched.
- No longer set OOF_CLK_DIS[x] based on user’s Precision & Fast OOF Enable checkbox. Now always set to 0 – similar to setting LOS_CLK_DIS=0 always – to work around RevA issue where corresponding FLG cannot be cleared unless OOF_CLK_DIS is 0.
- VCO frequency for Si5346/47 devices changed to 14.208 GHz. The frequency is now always listed in ’47 design reports. If you open a project using the old VCO frequency, your plan will be recalculated and you will be prompted to re-save your project file with the new Fvco.
- Added additional frequency selections to loop bandwidth combo boxes.
- Added new OID (Output Interpolative Divider) quantization spur design rule check.

New Rational Fraction Calculator:

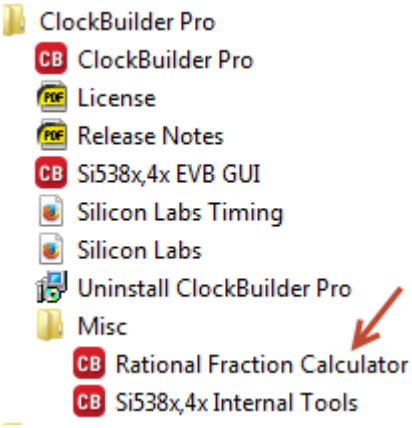
- Allows you to evaluate rational fraction expressions without loss of precision (as could be the case with a program like Microsoft Excel). Supports the same expression syntax used to define clock frequencies. For example:



- Launch from Wizard menu:



- Or Windows Start menu:



- Note pressing ENTER is a shortcut to the Calc button.

Version 1.0 [2014-07-30]

Initial release