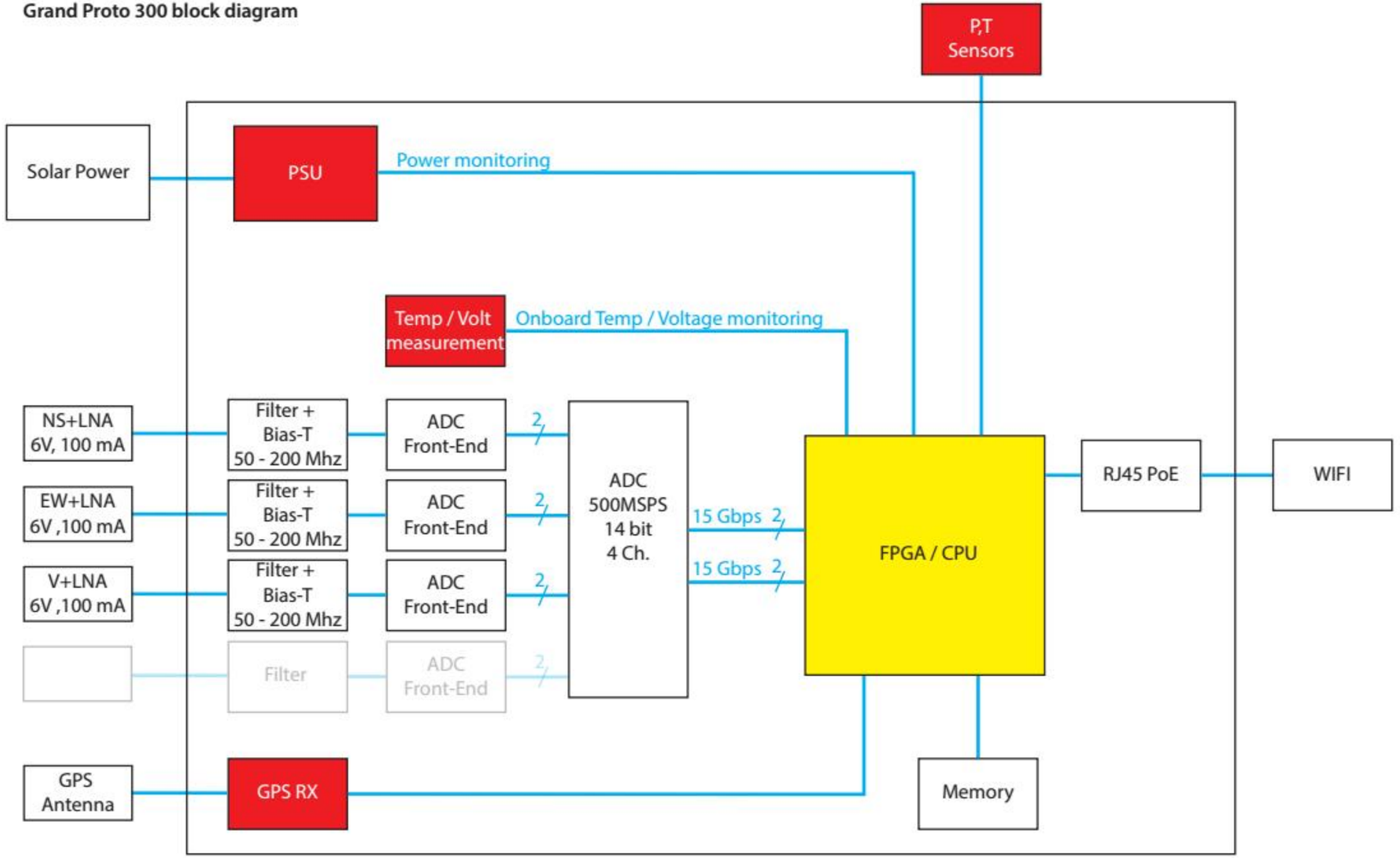
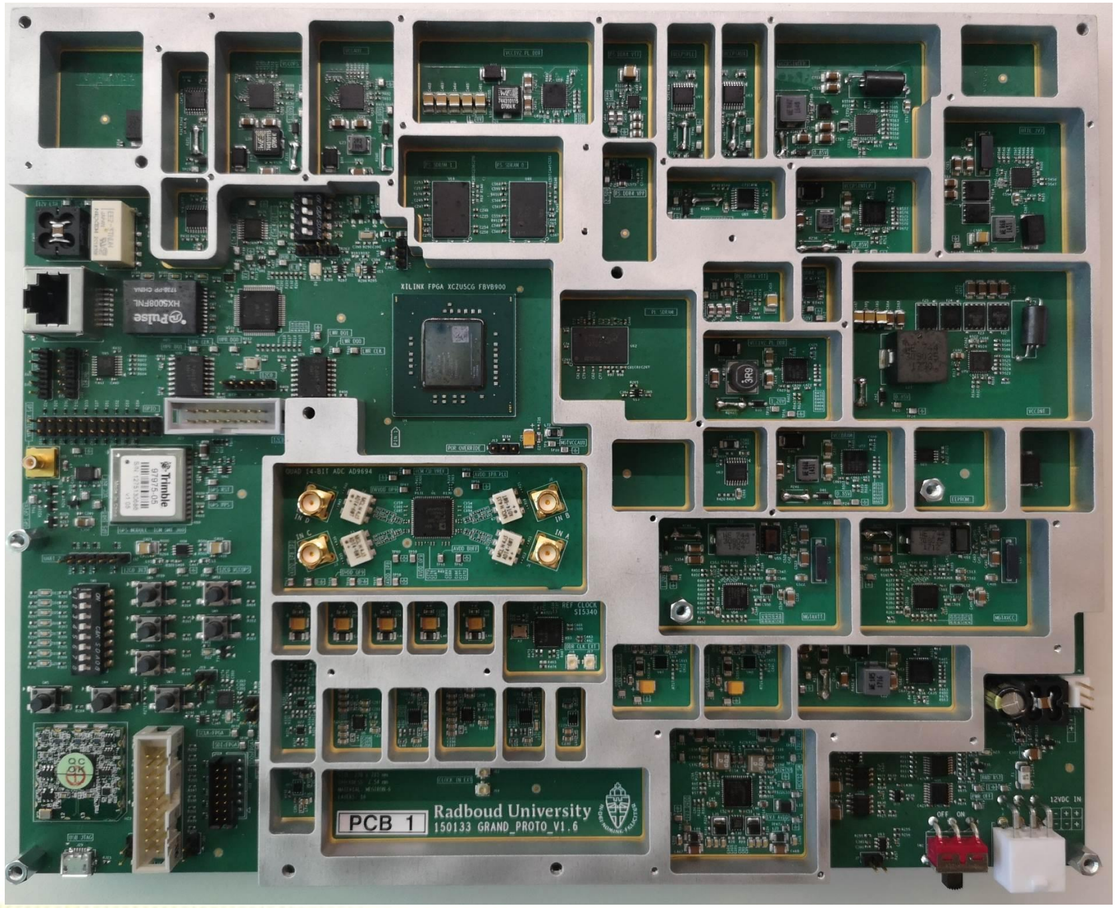
GRAND Status – Nijmegen

Front end, board design and firmware

Grand Proto 300 block diagram



GP300 Nijmegen board design – short overview

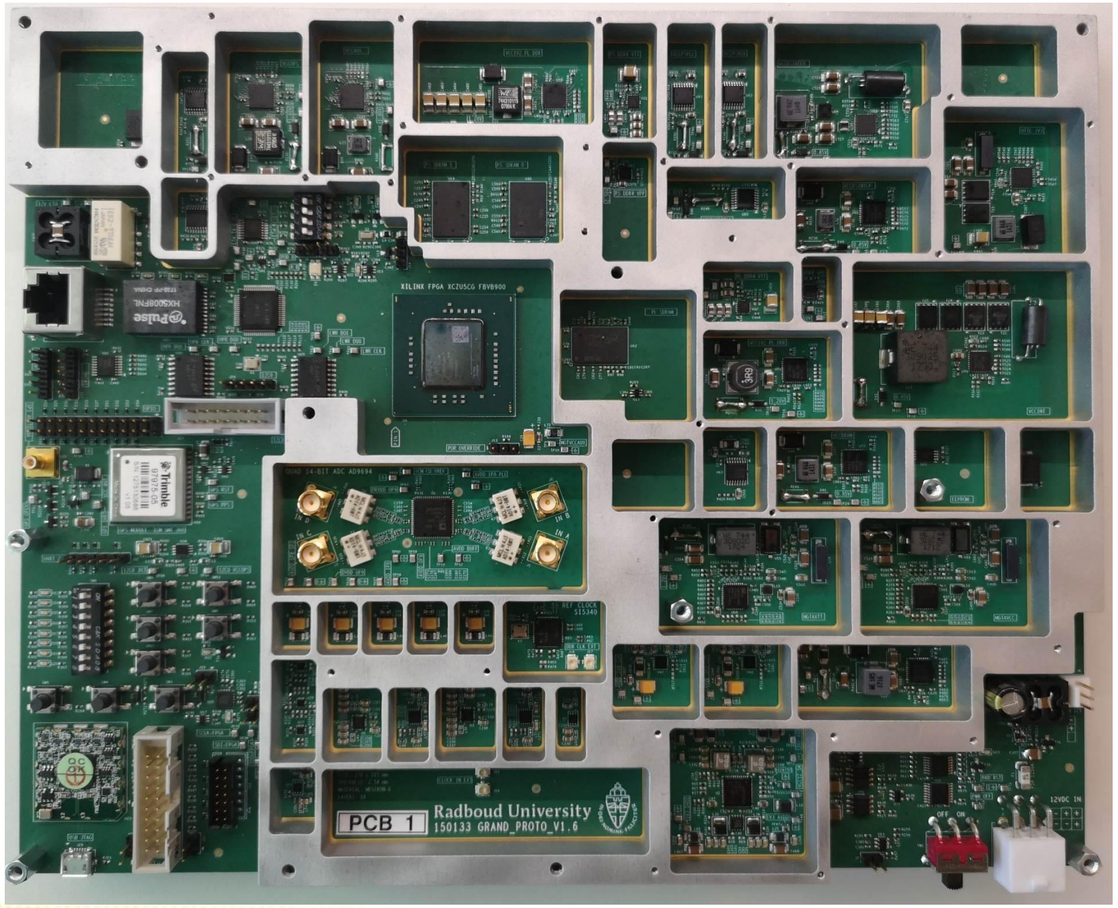


ZYNC ZU7EG SOC-FPGA
Application processor:
- Dual core Cortex A53, 1.5Ghz
Real-Time processor:
- Dual core Cortex R5, 600MHz
ADC
- AD9694 16 bit, 500MSPS
Low jitter clk
- Si5340, 90 fs rms jitter
20+ supplies

Highly configurable, on-line readout, low noise (for ADC and clock chip)

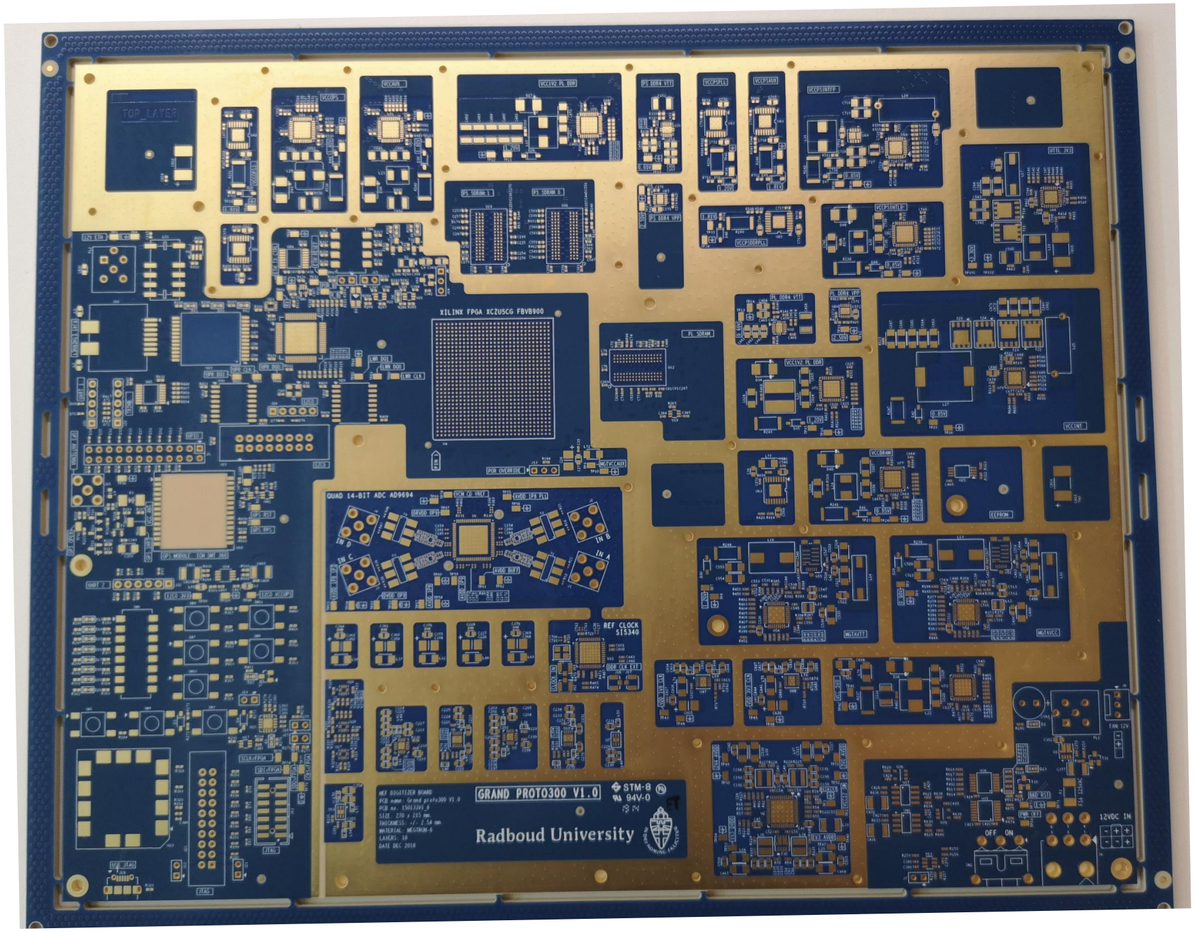
2 DDR4 interfaces
-1 GB, 32b interface connected to PS
-512 GB 16b interface connected to PL
10/100 Gb/s ethernet interface

GP300 Nijmegen board design - setbacks



Setbacks:
-Factory produced the board with preliminary files. (green PCB)
-Three supllies showed destructive oscilation after enabling output.
- Selected FPGA (XCZU5) was not available. An upgrade, the XCZU7, is used in stead.
-200+ components were not placed during production.
-Short between a ground via and a 1V8 power line in an internal layer of the board.

GP300 Nijmegen board design – current status



- All supllies are working and can be configured by software.
- Board is produced based on correct files and delivered to Nijmegen. (blue PCB)

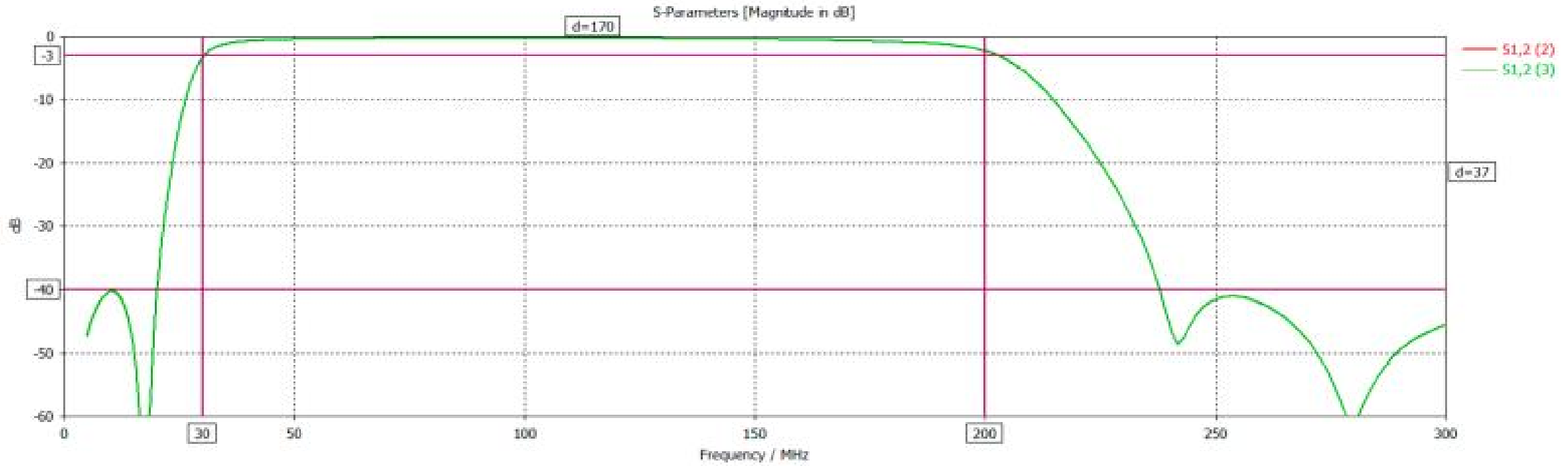
Coming weeks:
- Configure and test the clocks, JTAG, I2C and SPI.
- Continue with firmware design and start implementation.

Status filter design

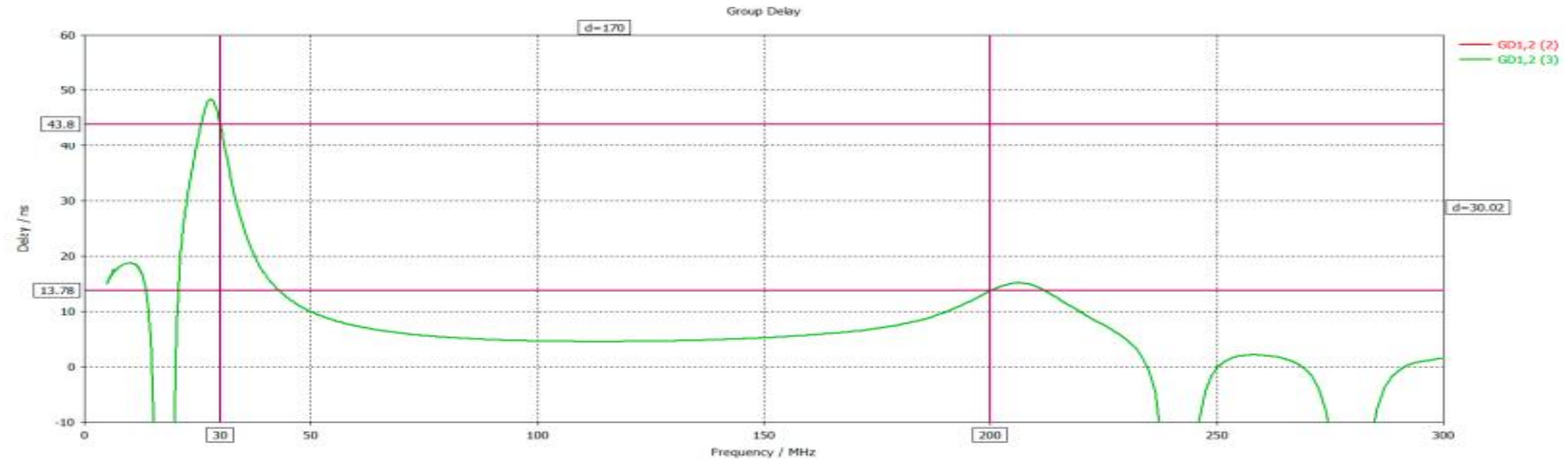
- Filter design is finished
- Fine-tuning done with real components

Next step:
- Create test board and measure filter performance

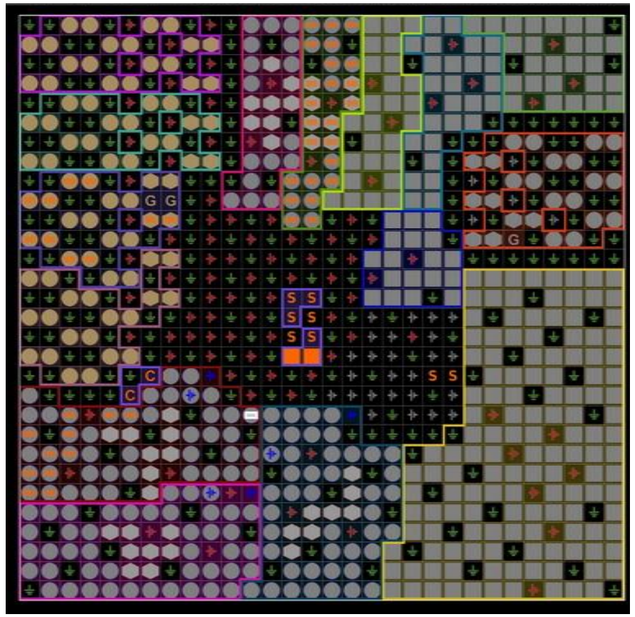
S2,1 simulated with real components:



Group Delay(1,2) simulated with real components:



Status firmware and software



Firmware

Until the prototype is fully operational all firmware is developed for the Xilinx reference board.

- High speed ADC readout (JESD204B interface) is finished but needs a Linux kernel to be up and running to be able to test functionality. Kernel image is build but hangs during boot. **Needs debugging.**

- Firmware for DDR4 memory test (PL-side) is build. **Needs modified clock chip setup.**

- Firmware for triggering and data packaging is available but must be copied and modified from the previous Auger digitizer. **Needs to be started.**

Processor system / Software

Basic Linux kernel can be build and loaded in Xilinx ref board.

To do:

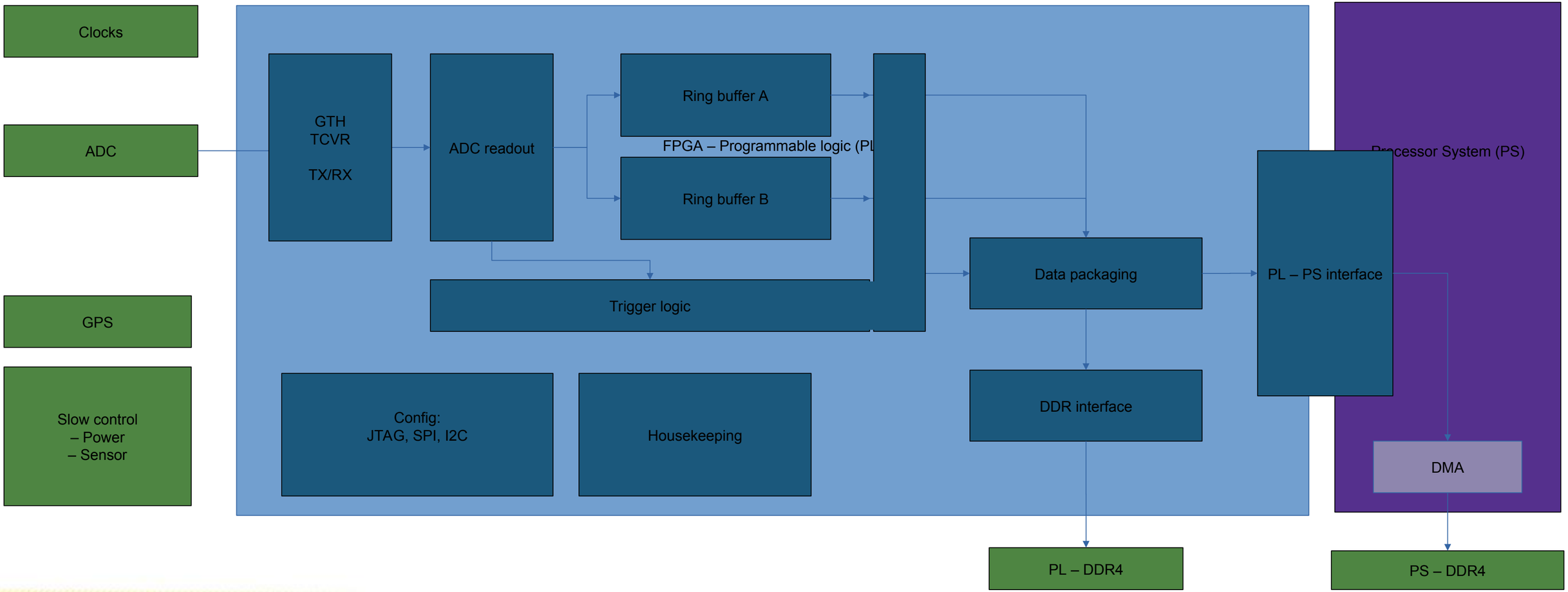
- include ADC readout in kernel

- interface to memories

- migration software Auger digitizer

- readout sensors (pressure, humidity and temperature)

Firmware setup



Start / Stop address	Partition name	Size [Bytes, hex]	Size [Bytes, decimal]
0x0 0x1e00000	boot	0x1e00000	31457280
0x1e00000 31457280 0x1e40000 31719424	bootenv	0x40000	262144
0x1e40000 31719424 0x4240000 69468160	kernel	0x2400000	37748736
0x4240000 0x452F24F8	jffs2	0x2EAF0B8 0x2EF0000	50000000 (50MB) 49217536 (49MB)
0x7130000 118685696 0x7140000	spare	0x10000	65536
Total used			119.468.160 (955745280 bits)
Total available 748 ste bytes [MiB] = 1.073 741 824 bits = 2x 512Mb		0x7735940	125MB (1Gbit)

Flash memory size must be multiples of 65636 bytes → 0x10000

QSPI boot setup

Volg:
https://wiki.analog.com/resources/tools-software/linux-build/generic/petalinux

petalinux-create -t project --template zynqMP --name QSPI13mrt
> cd QSPI13mrt/
> petalinux-config --get-hw-description=/home/rene/Data/FPGA_workdir/adi/hdl/projects/daq3/zcu102/daq3_zcu102.sdk
→ Subsystem AUTO Hardware Settings → Memory Settings
System memory size = 0x37fffffff

→ Subsystem AUTO Hardware Settings → Flash Settings
Primary Flash (psu_qspi_0) --->
[ ] Advanced Flash Auto Configuration
*** partition 0 ***
(boot) name
(0x1e00000) size
*** partition 1 ***
(bootenv) name
(0x40000) size
*** partition 2 ***
(kernel) name
(0x2400000) size
*** partition 3 ***
(jffs2) name
(0x2EE0000) size
*** partition 4 ***
(spare) name
(0x20000) size
*** partition 5 ***
() name

→ Subsystem AUTO Hardware Settings → Advanced bootable images storage Settings → boot image settings
image storage media = (X) primary flash

→ Subsystem AUTO Hardware Settings → Advanced bootable images storage Settings → kernel image settings
image storage media = (X) primary flash

→ Image Packaging Configuration
Root filesystem type = (X) JFFS2
jffs2 erase block size(KByte) = (X) jffs2 erase block size: 128KiB

→ Yocto Settings → User Layers
(/home/rene/Data/FPGA_workdir/adi/meta-adi/meta-adi-core) user layer 0
(/home/rene/Data/FPGA_workdir/adi/meta-adi/meta-adi-xilinx) user layer 1

Edit system-conf.dtsi to resemble flash partition and disable SD card:
/include/ "system-conf.dtsi"
/ {
};

&sdhci1 {
status = "disabled";
};

&qspi {
status = "okay";
is-dual = <1>;
has-io-mode = <1>;
/delete-node/ flash@0;
flash@0 {
compatible = "micron,m25p80", "spi-flash", "n25q512a"; /* dual 512Mb, 1Gb total */
#address-cells = <0x1>;
#size-cells = <0x1>;
reg = <0x0>;
spi-tx-bus-width = <0x1>;
spi-rx-bus-width = <0x4>;
spi-max-frequency = <0x66ff300>;
partition@boot {
label = "boot";
reg = <0x0 0x1e00000>;
};

partition@bootenv {
label = "bootenv";
reg = <0x1e00000 0x40000>;
};

partition@kernel {
label = "kernel";
reg = <0x1e40000 0x2400000>;
};

partition@jffs2 {
label = "jffs2";
reg = <0x4240000 0x2EE0000>;
};
partition@spare {
label = "spare";
reg = <0x7120000 0x20000>;
};
};
};

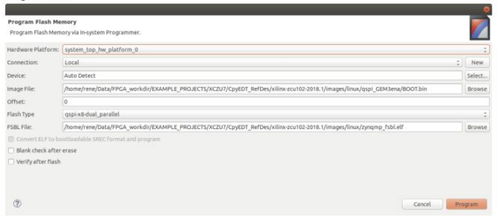
Edit kernel setting for default erase size of flash following: https://forums.xilinx.com/t5/Embedded-Linux/mount-jffs2-filesystem-error/td-p/843748
> petalinux-config -c kernel
device driver -> memory technology device(MTD) support -> SPI-NOR device support -> Use small 4096 B erase sectors
uncheck!
(default config is checked.)

> petalinux-build
> petalinux-package --boot --fsbl --fpga --u-boot --kernel --add images/linux/rootfs.jffs2 --offset 0x4240000 --force

Program BOOT.BIN with sdk gui.
> source /opt/Xilinx/Vivado/2018.3/settings64.sh
> xsdk

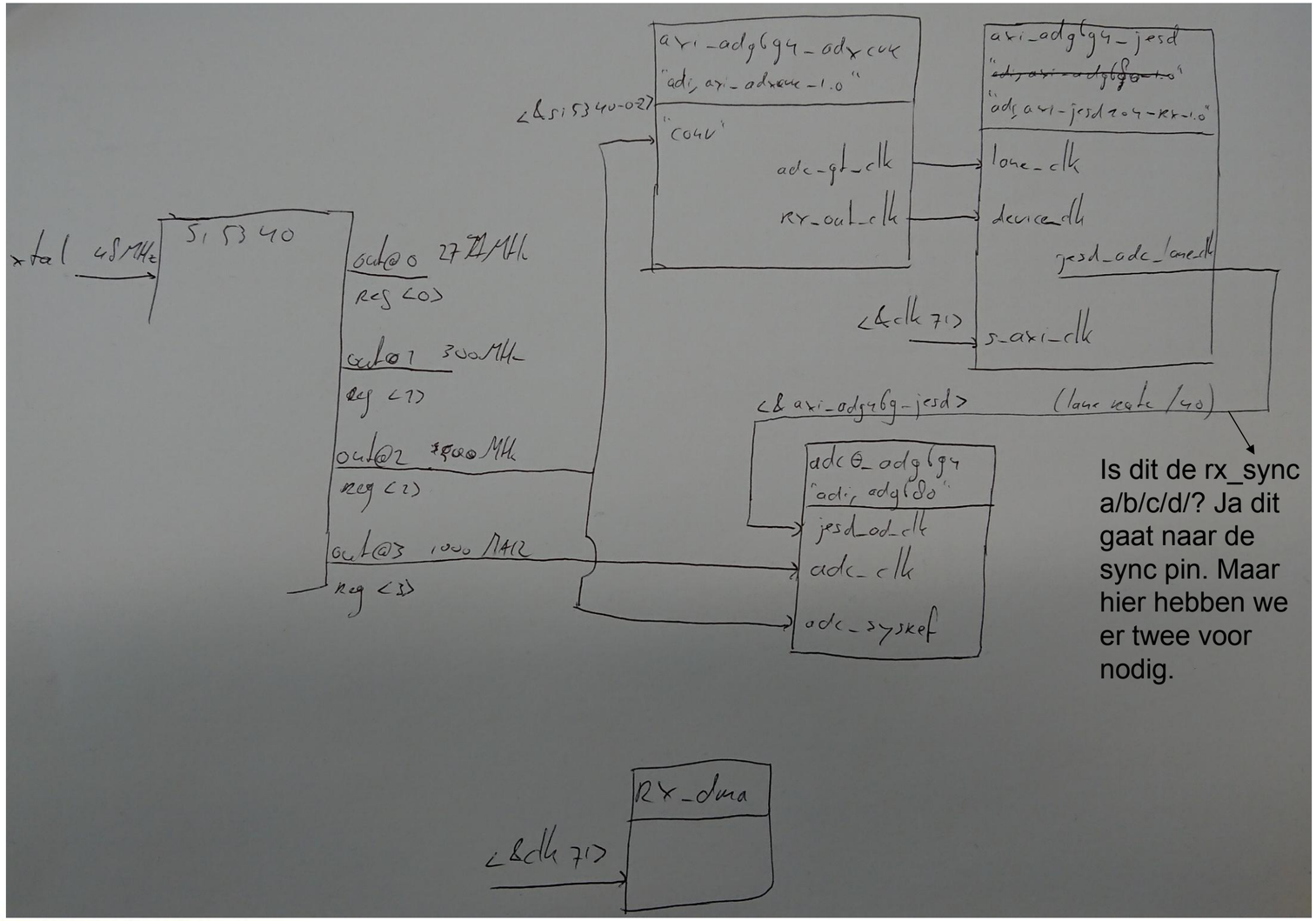
set boot mode to 0000 jtag boot
Alle schakelaars van grand moeten naar naar boven staan, oftwel weg van de cijfers op de bootschakelaar.

Program flash



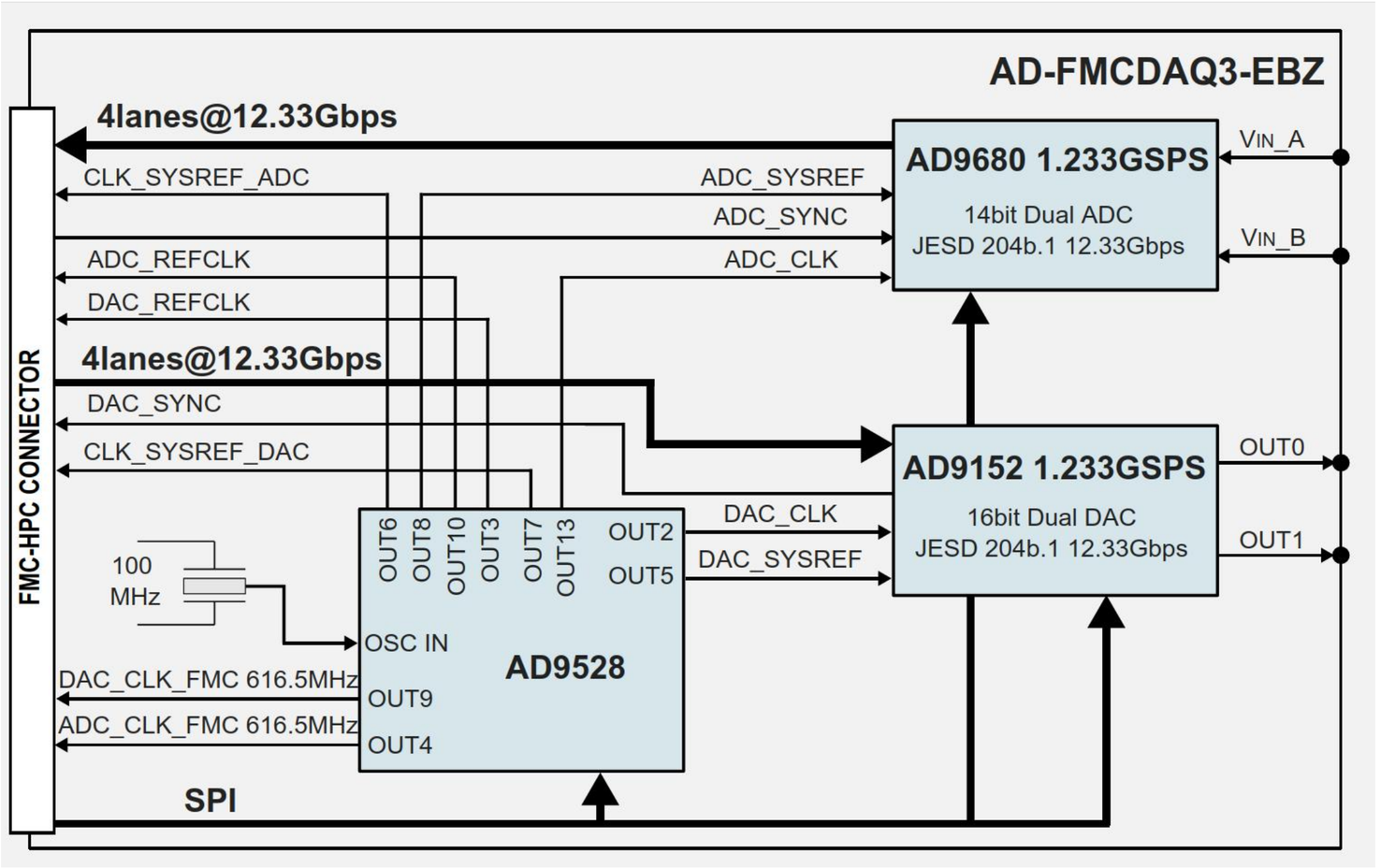
set boot mode to 0000 qspi boot
Schakelaar van grand moet bij "3" naar beneden staan, de andere schakelaars moet weg van de cijfers.

Thank you for your attention



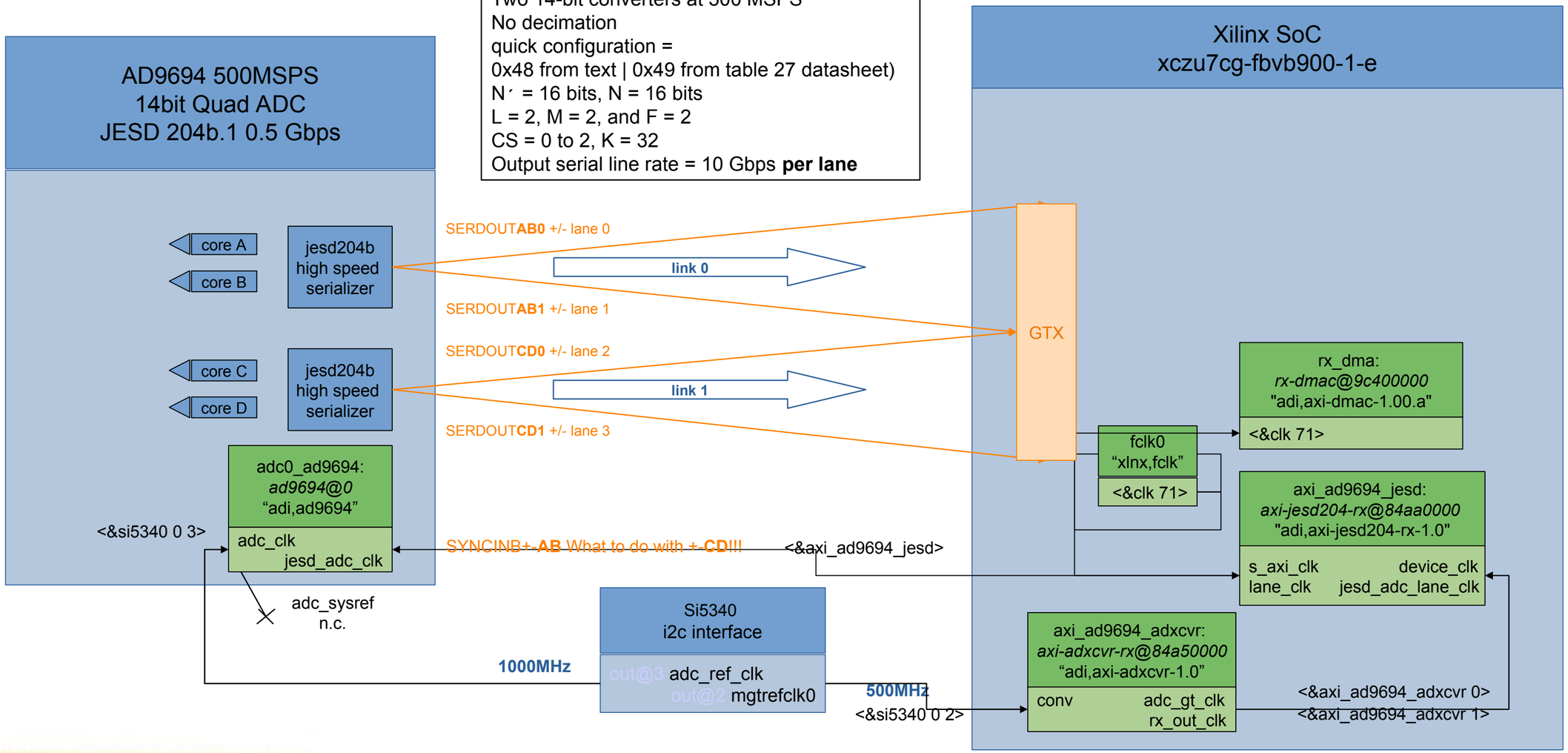
Is dit de rx_sync a/b/c/d/? Ja dit gaat naar de sync pin. Maar hier hebben we er twee voor nodig.

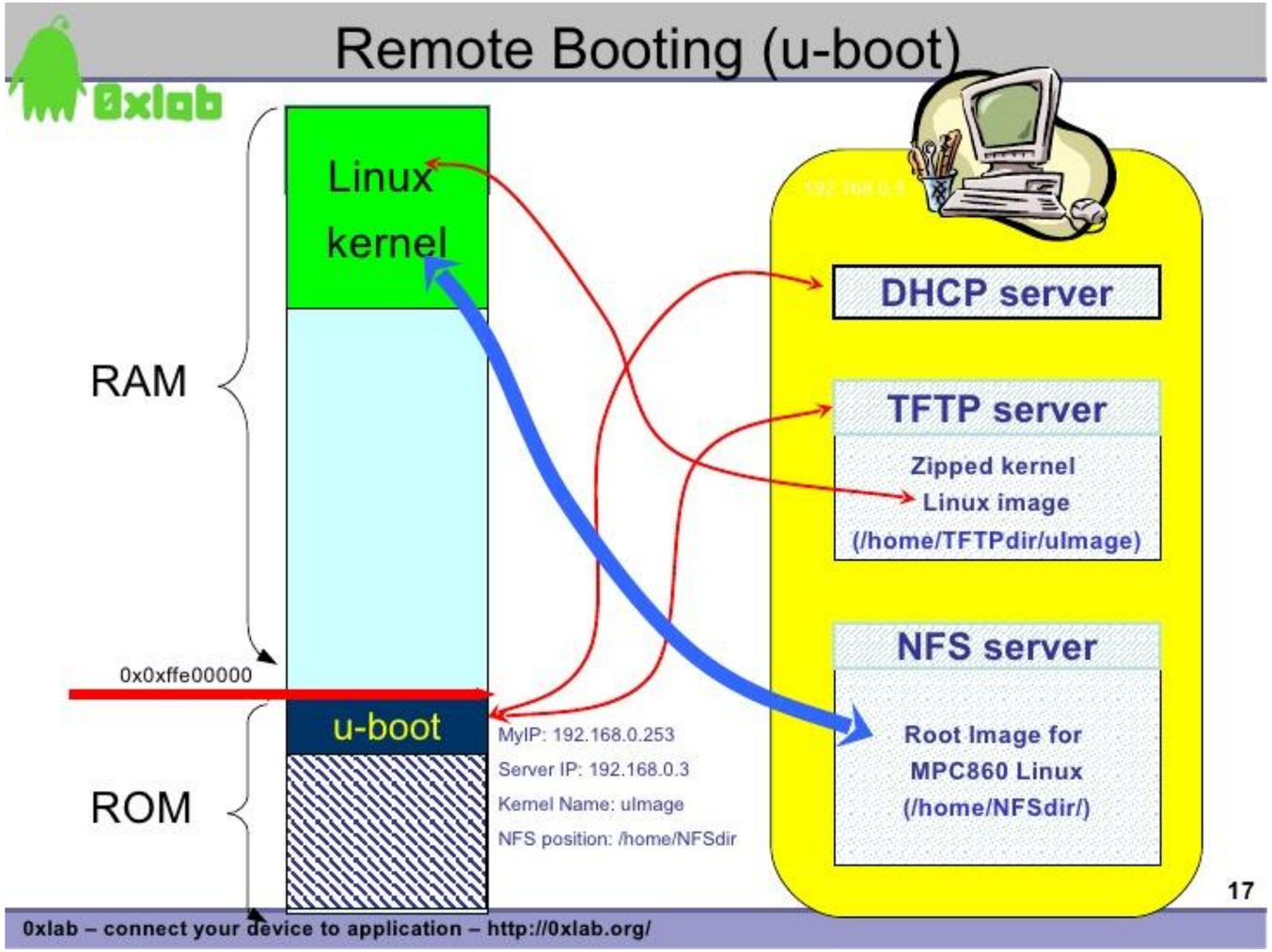
Backup slides


AD-FMCDAQ3-EBZ
4lanes@12.33Gbps
AD9680 1.233GSPS
14bit Dual ADC
JESD 204b.1 12.33Gbps
VIN_A
VIN_B
CLK_SYSREF_ADC
ADC_SYSREF
ADC_SYNC
ADC_REFCLK
ADC_CLK
DAC_REFCLK
FMC-HPC CONNECTOR
4lanes@12.33Gbps
DAC_SYNC
CLK_SYSREF_DAC
AD9152 1.233GSPS
16bit Dual DAC
JESD 204b.1 12.33Gbps
OUT0
OUT1
DAC_CLK
DAC_SYSREF
OUT6
OUT8
OUT10
OUT3
OUT7
OUT13
OUT2
OUT5
100
MHz
OSC IN
AD9528
DAC_CLK_FMC 616.5MHz
OUT9
ADC_CLK_FMC 616.5MHz
OUT4
SPI

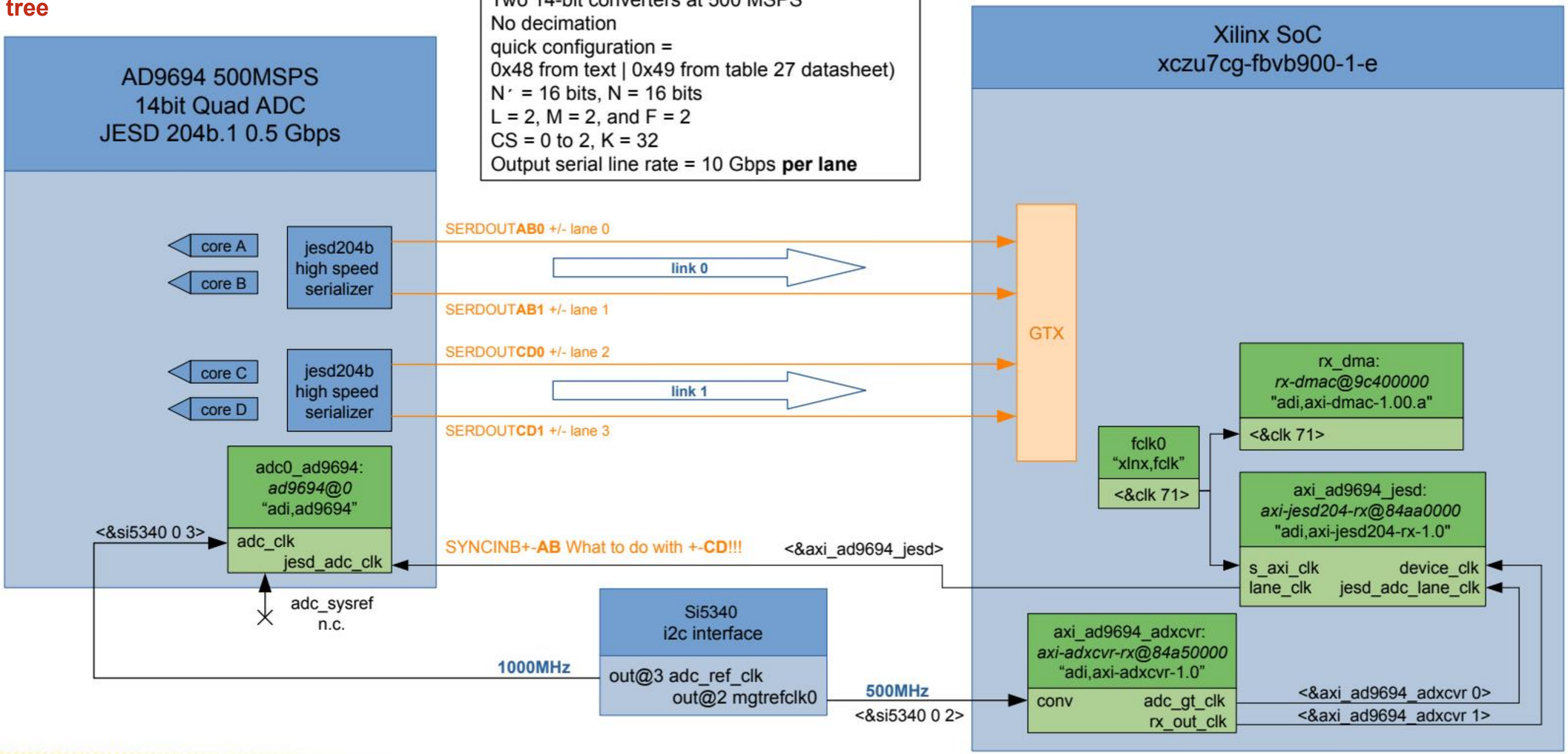
Linux device tree

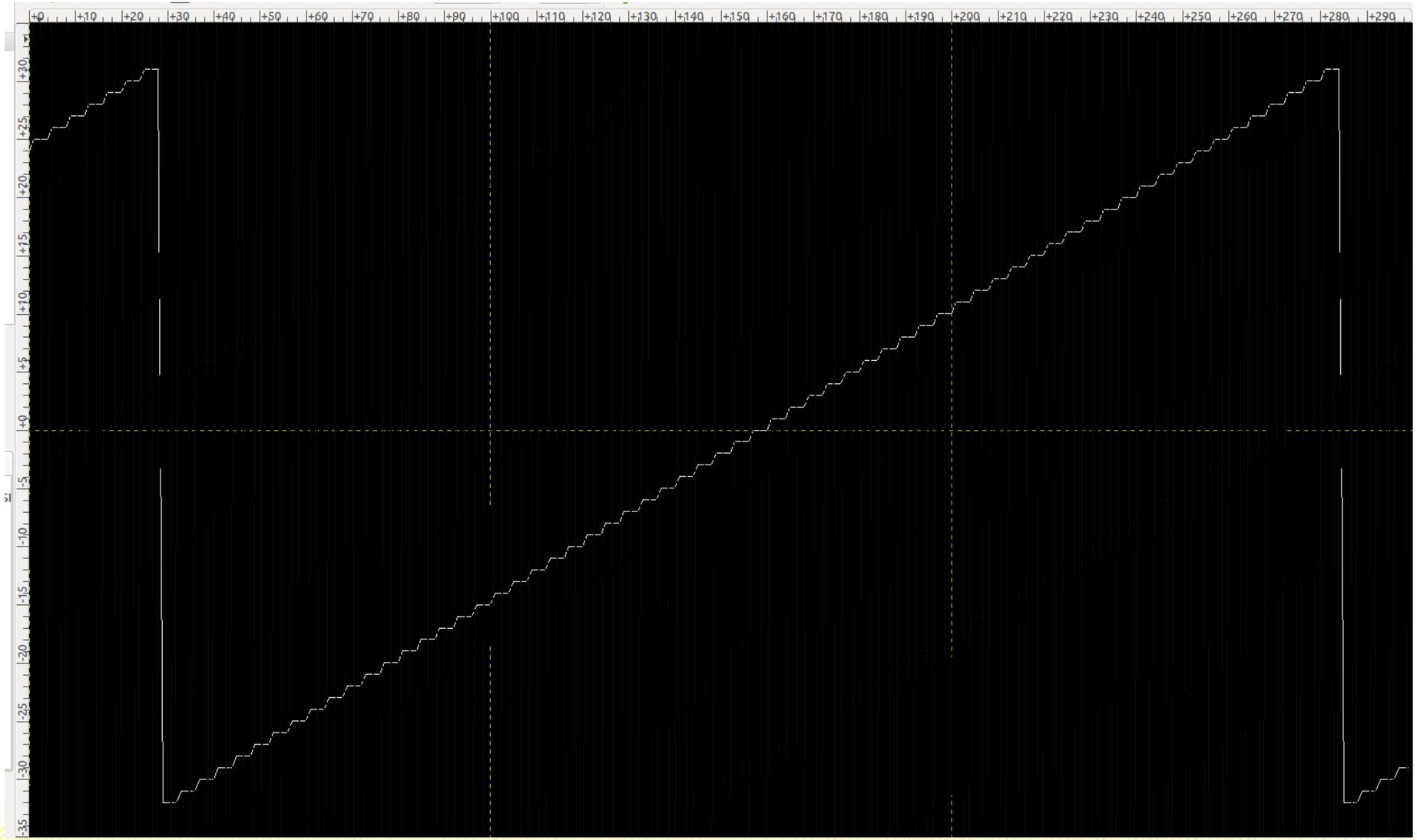
Per LINK! – full BW mode
Two 14-bit converters at 500 MSPS
No decimation
quick configuration =
0x48 from text | 0x49 from table 27 datasheet)
N´ = 16 bits, N = 16 bits
L = 2, M = 2, and F = 2
CS = 0 to 2, K = 32
Output serial line rate = 10 Gbps **per lane**

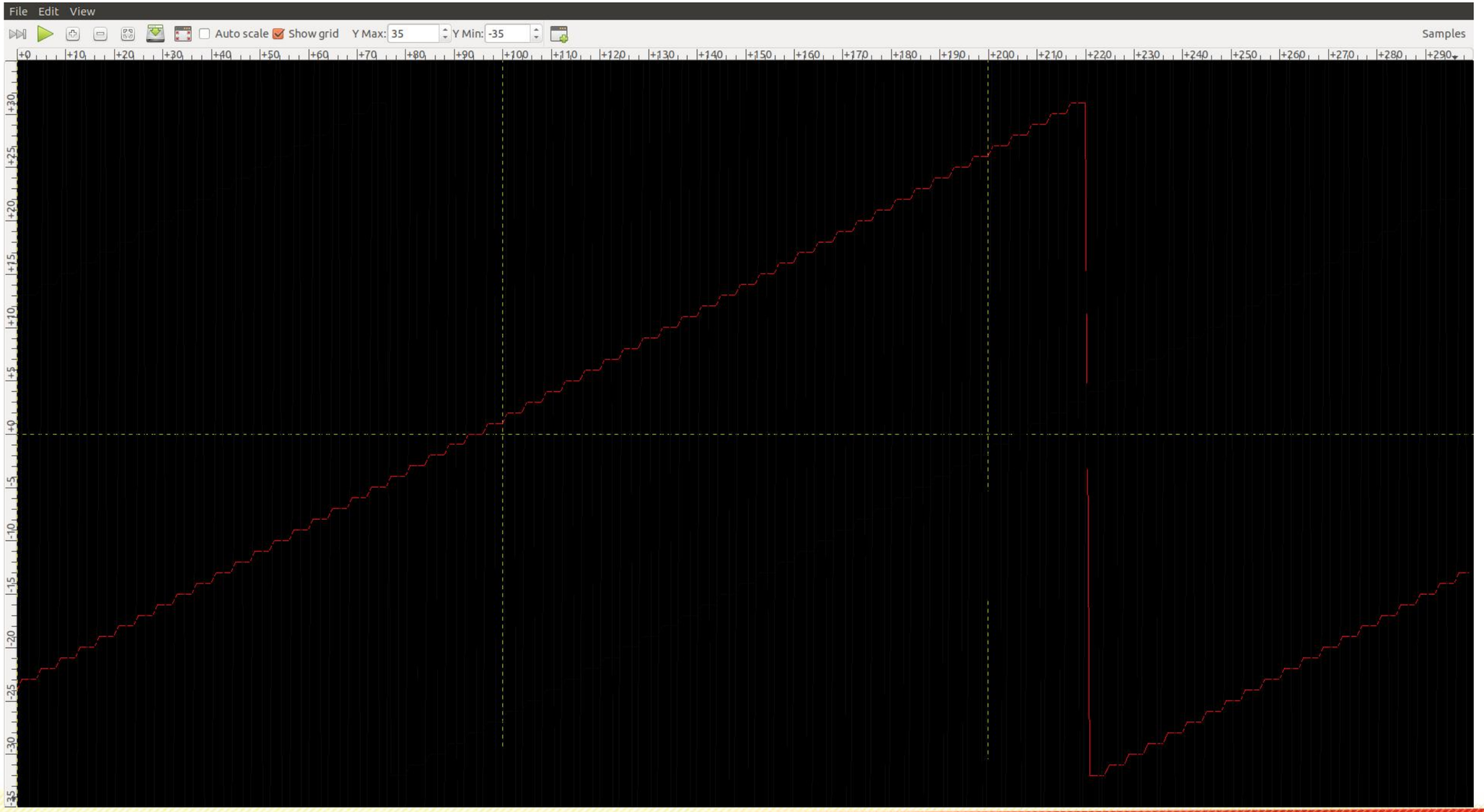


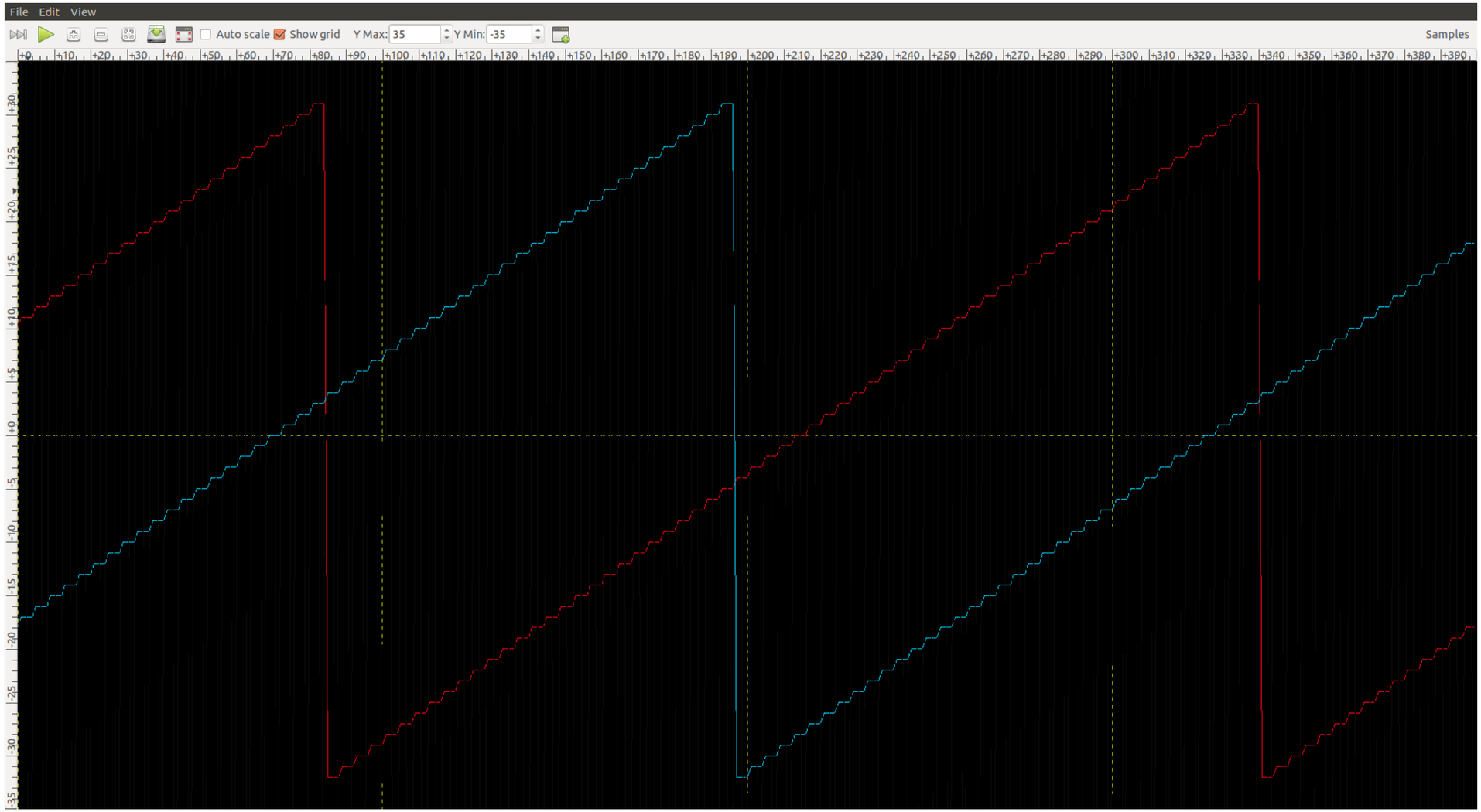

Remote Booting (u-boot)
0xlab
Linux kernel
RAM
0x0xffe00000
u-boot
ROM
MyIP: 192.168.0.253
Server IP: 192.168.0.3
Kernel Name: uImage
NFS position: /home/NFSdir
DHCP server
TFTP server
Zipped kernel Linux image (/home/TFTPdir/uImage)
NFS server
Root Image for MPC860 Linux (/home/NFSdir/)
17
0xlab – connect your device to application – http://0xlab.org/

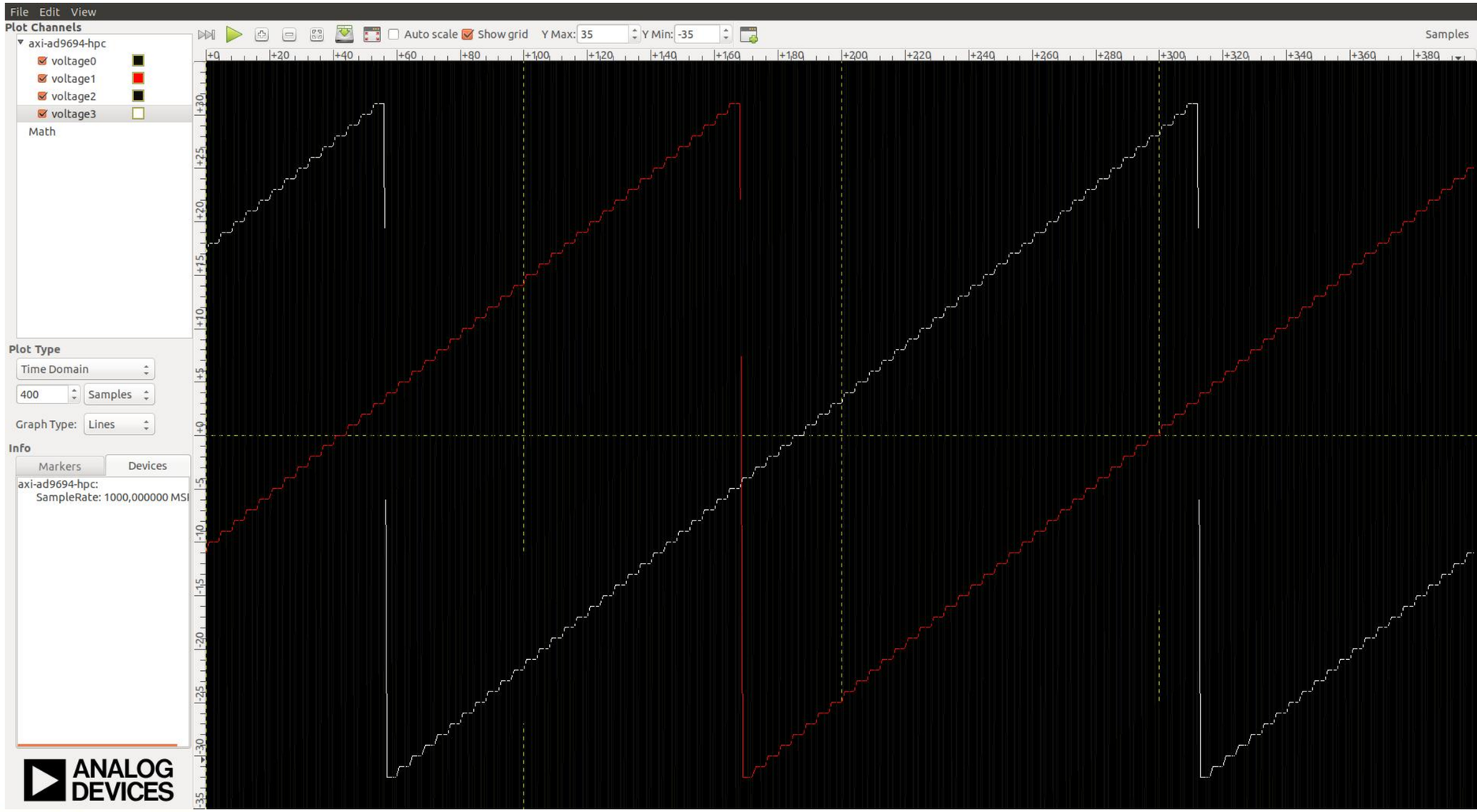
Clock config
– Linux device tree

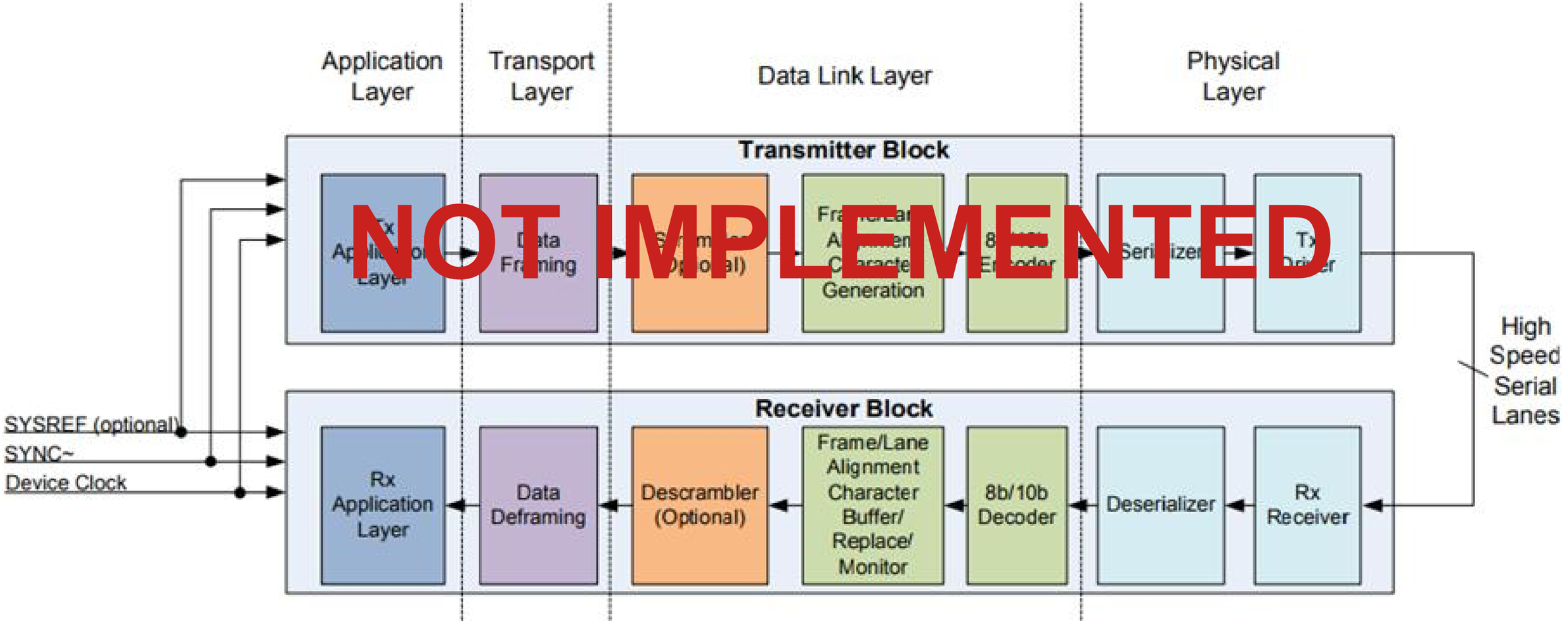



+0 +10 +20 +30 +40 +50 +60 +70 +80 +90 +100 +110 +120 +130 +140 +150 +160 +170 +180 +190 +200 +210 +220 +230 +240 +250 +260 +270 +280 +290
+35 +30 +25 +20 +15 +10 +5 +0 -5 -10 -15 -20 -25 -30 -35


File Edit View
Auto scale
Show grid
Y Max: 35
Y Min: -35
Samples
+0 +10 +20 +30 +40 +50 +60 +70 +80 +90 +100 +110 +120 +130 +140 +150 +160 +170 +180 +190 +200 +210 +220 +230 +240 +250 +260 +270 +280 +290
+30 +25 +20 +15 +10 +5 +0 -5 -10 -15 -20 -25 -30 -35


File Edit View
Auto scale
Show grid
Y Max: 35
Y Min: -35
Samples


File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 35
Y Min: -35
Samples
Plot Type
Time Domain
400
Samples
Graph Type: Lines
Info
Markers
Devices
axi-ad9694-hpc:
SampleRate: 1000,000000 MSI
ANALOG DEVICES



NOT IMPLEMENTED

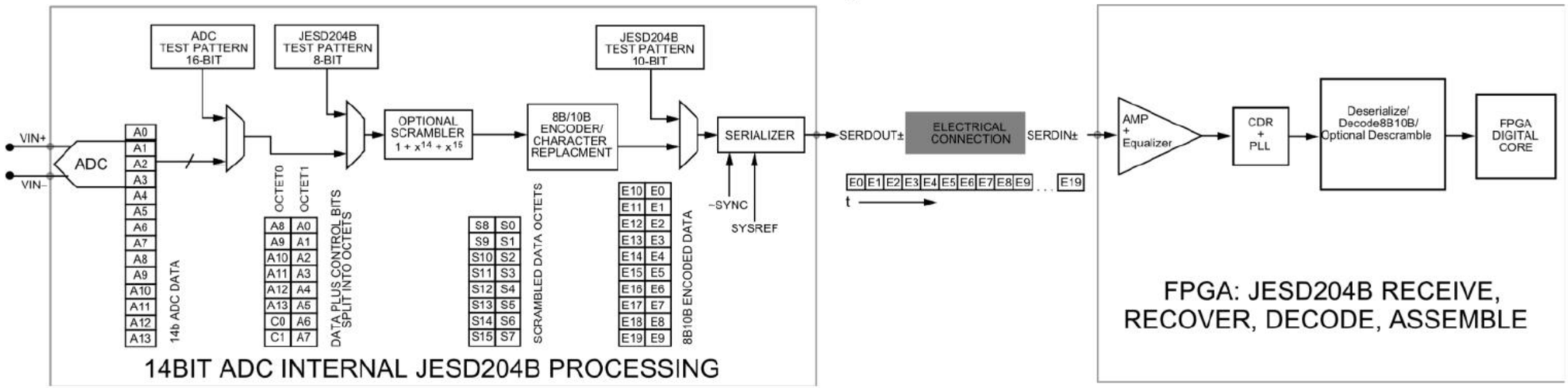
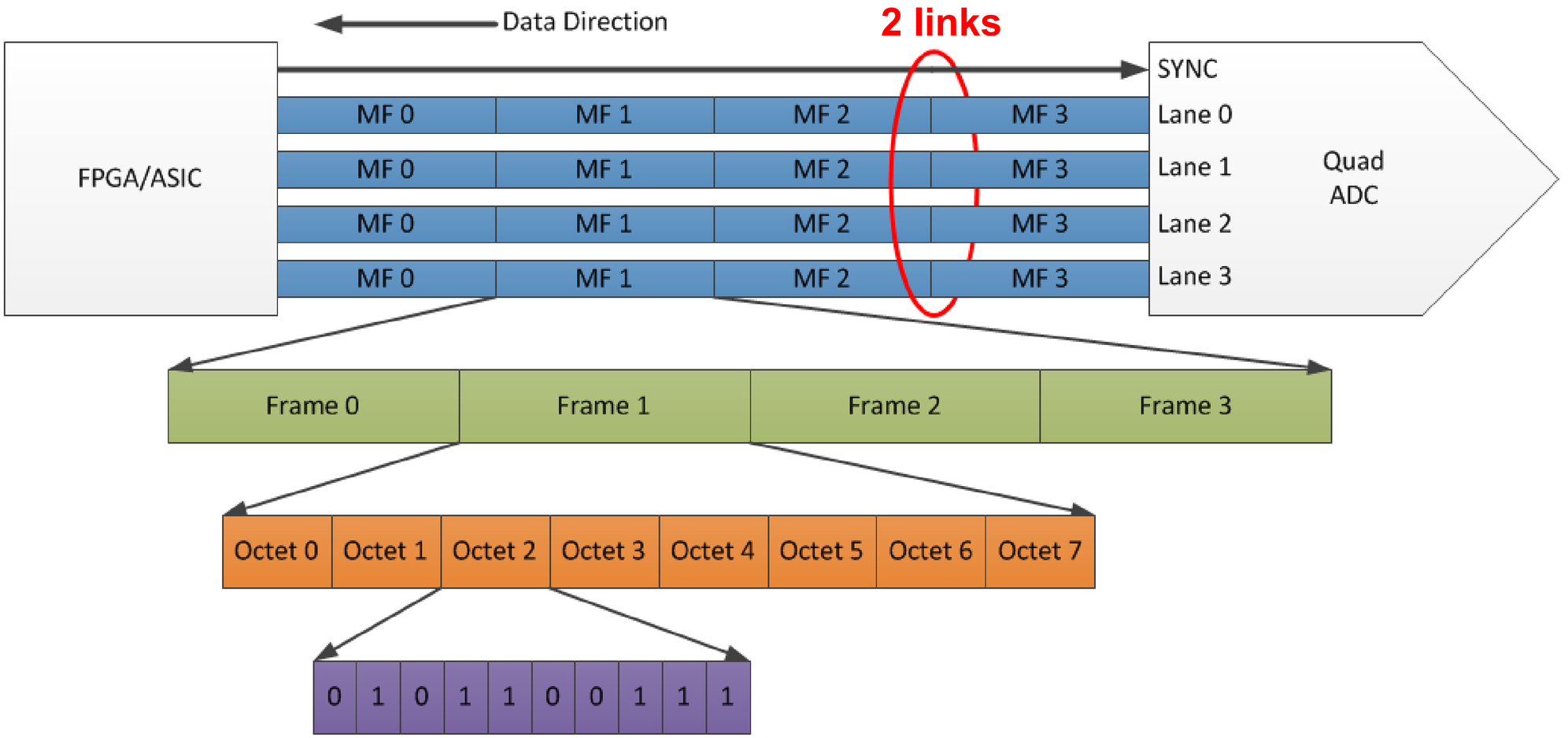
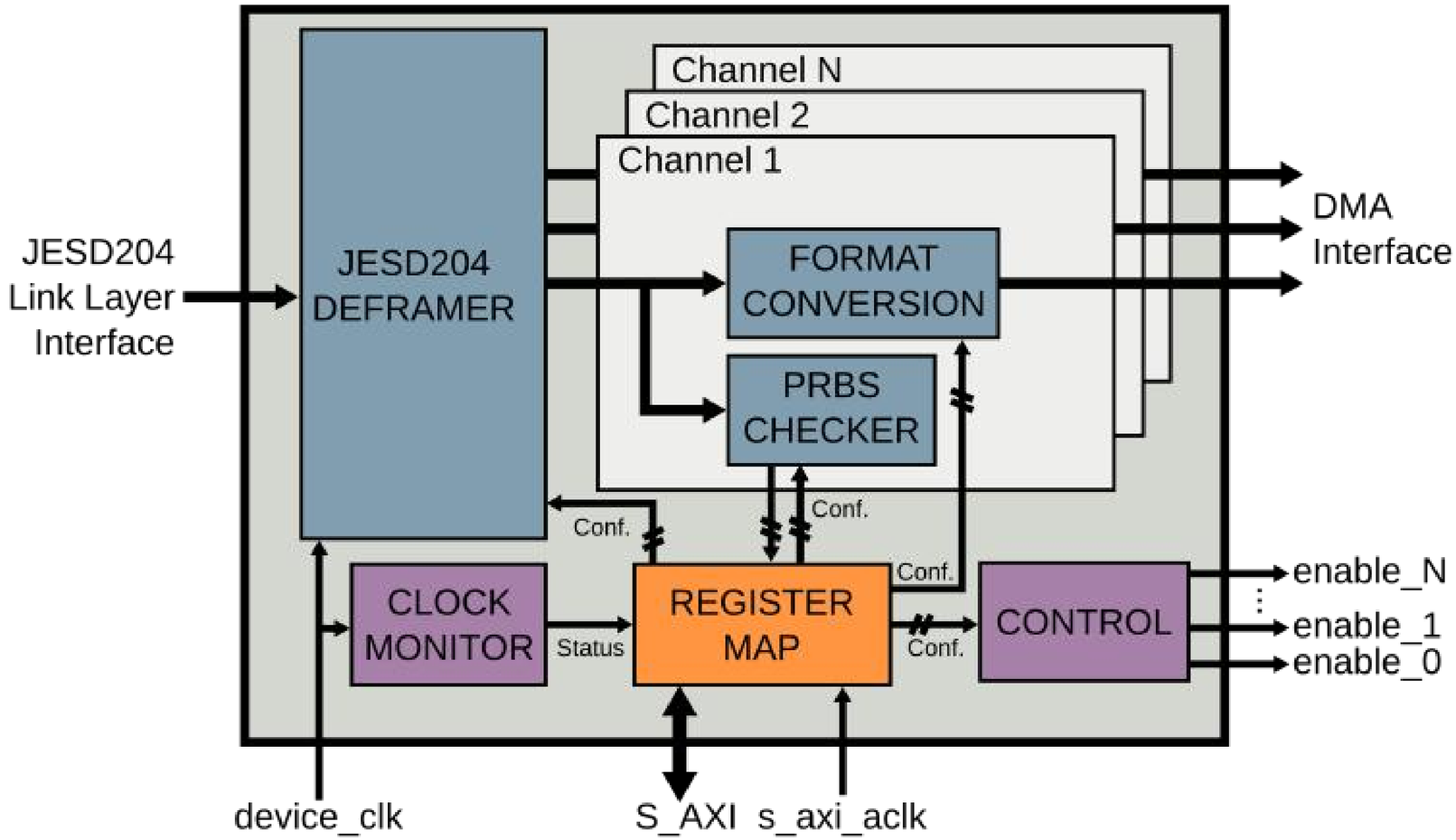


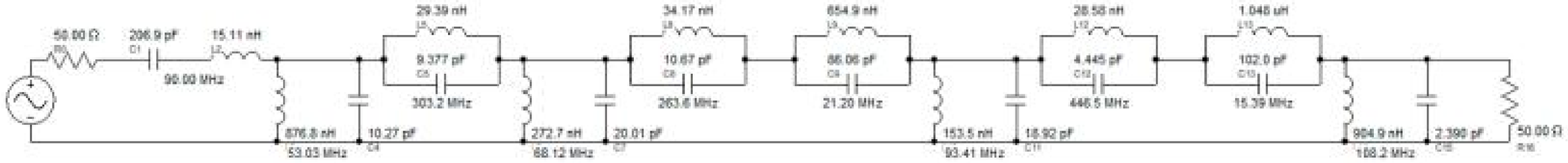
Figure 1. JESD204B Link Diagram for One ADC to an FPGA through One Lane


Data Direction
2 links
FPGA/ASIC
SYNC
Lane 0
Lane 1
Lane 2
Lane 3
Quad
ADC
MF 0
MF 1
MF 2
MF 3
Frame 0
Frame 1
Frame 2
Frame 3
Octet 0
Octet 1
Octet 2
Octet 3
Octet 4
Octet 5
Octet 6
Octet 7
0 1 0 1 1 0 0 1 1 1


JESD204
Link Layer
Interface
JESD204
DEFRAMER
Channel N
Channel 2
Channel 1
FORMAT
CONVERSION
PRBS
CHECKER
DMA
Interface
Conf.
Conf.
Conf.
CLOCK
MONITOR
Status
REGISTER
MAP
Conf.
CONTROL
enable_N
enable_1
enable_0
device_clk
S_AXI
s_axi_aclk

Status filter design

Schematic with ideal components:



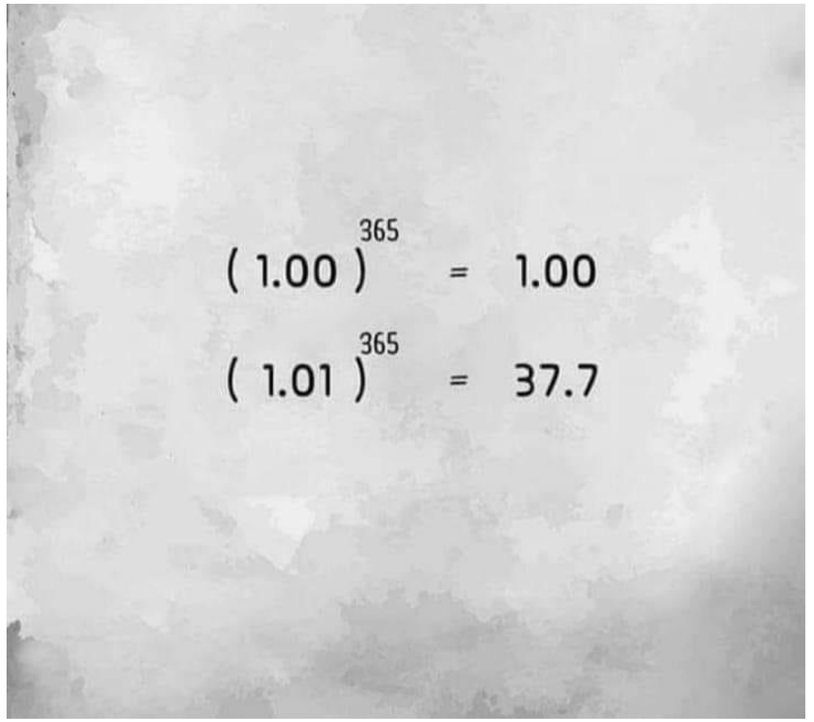
"From small debugging steps to a GRAND result"

What happened
- Combine Xilinx design with Analog Devices design
- boot from QSPI / flash partion table
- Modifiy board files Xilinx
- Search best firmware base to start from
- Change firmware Analog Devices hdl repo
- Yocto design flow
- Modify device tree where are they and how to change them. Overlays/includes are a great help and a great pain. Easy to get the device tree but difficult to modify and use them
- Boot linux
- Add missing device drivers, mainly clock
- Debug axi busses, ADC setting and JESD204 lane setting
- Combine everything in git.
- Clean up and remove unused functionality
- 25-3 first boot without adc and clock driver but with qspi and AD device tree. (started ticket)
- 6-5 first answer Analog Devices
- 30-6 NFS boot and send mail to CIC>EMEA@analog.com (helpdesk)
- 7-7 follow up from Analog Devices
- 13-7 first signals in IIO scope
- 23-7 4 ramp signals in IIO scope

Tips, lessons learned
- Select you Analog devices HDL project based on available device drivers.
- Learn git
- Invest time in development environment especially when booting from QSPI memory. Test it and forget it.Switch to NFS boot as soon as possible. Quite some time spent on gettign the boot arguments correct for NFS boot
- Email Analog Devices to ask for priority on ticket.
- Learn how to do apply a patch (in GIT and add this patch in Yocto, with a patch you can also add source code.

Open items
- Using QEMU seems to work out of the box but ran into difficulties with the QSPI boot. Could potentially save a lot of time with testing device drivers and boot
- Petalinux-build mrproper modifiying the device tree and perform:

$ petalinux-build -c device-tree -x cleansstate
$ petalinux-build -c device-tree
Build the device tree but does not result in a bootable image for the QSPI boot.



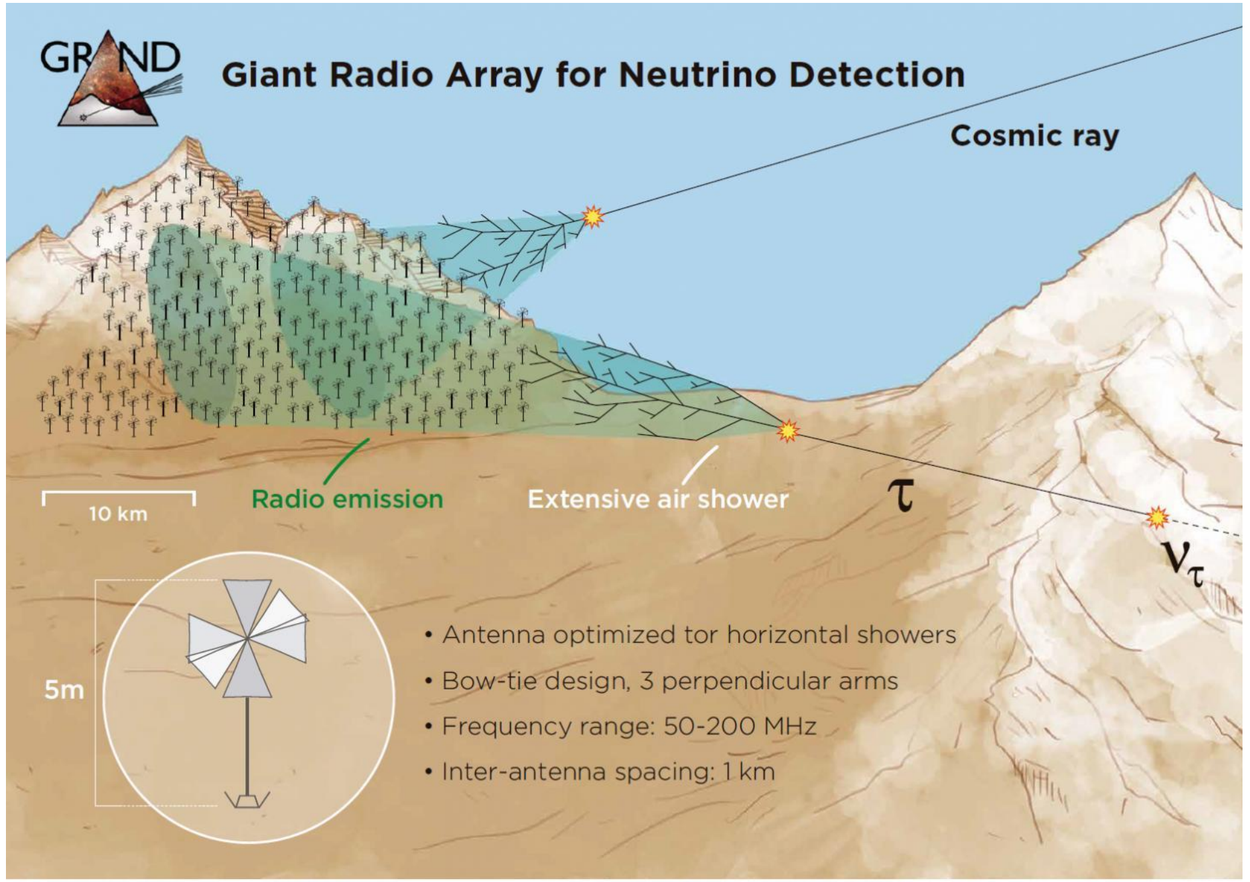
GRAND – Giant Radio Array for Neutrino Detection

Initiative of Olivier Martineau (scientist: LPNHE)
Group in Nijmegen working on GRAND

Department: High Energy Physics
– Sijbrand de Jong

GRAND:
– Charles Timmermans (scientist: Nikhef)
– Dániel Szálas-Motesiczky (engineer: RU)
– Floris Hahn (PCB designer: Techno Center, RU)

– René Habraken (engineer: RU)
r.habraken@science.ru.nl

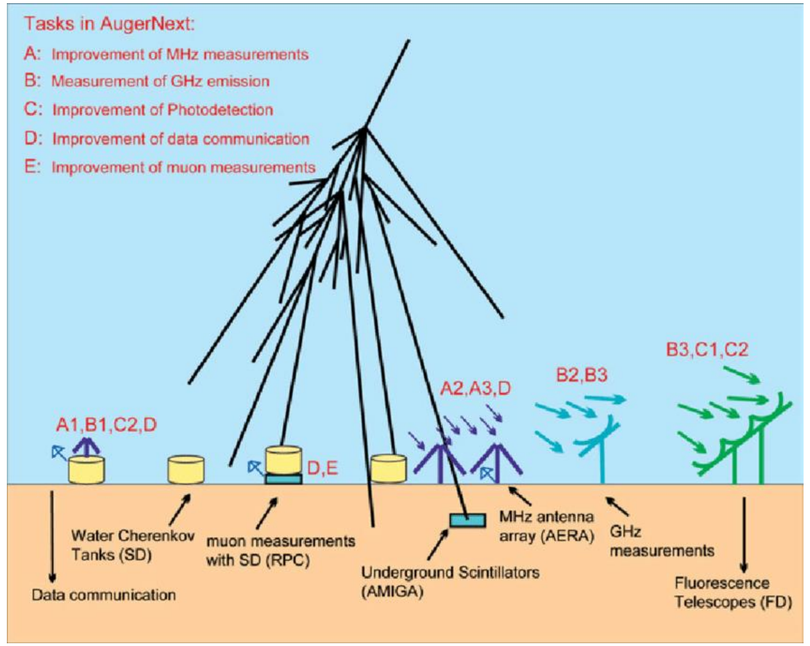


AERA

– *Electronics Auger Engineering Radio Area*

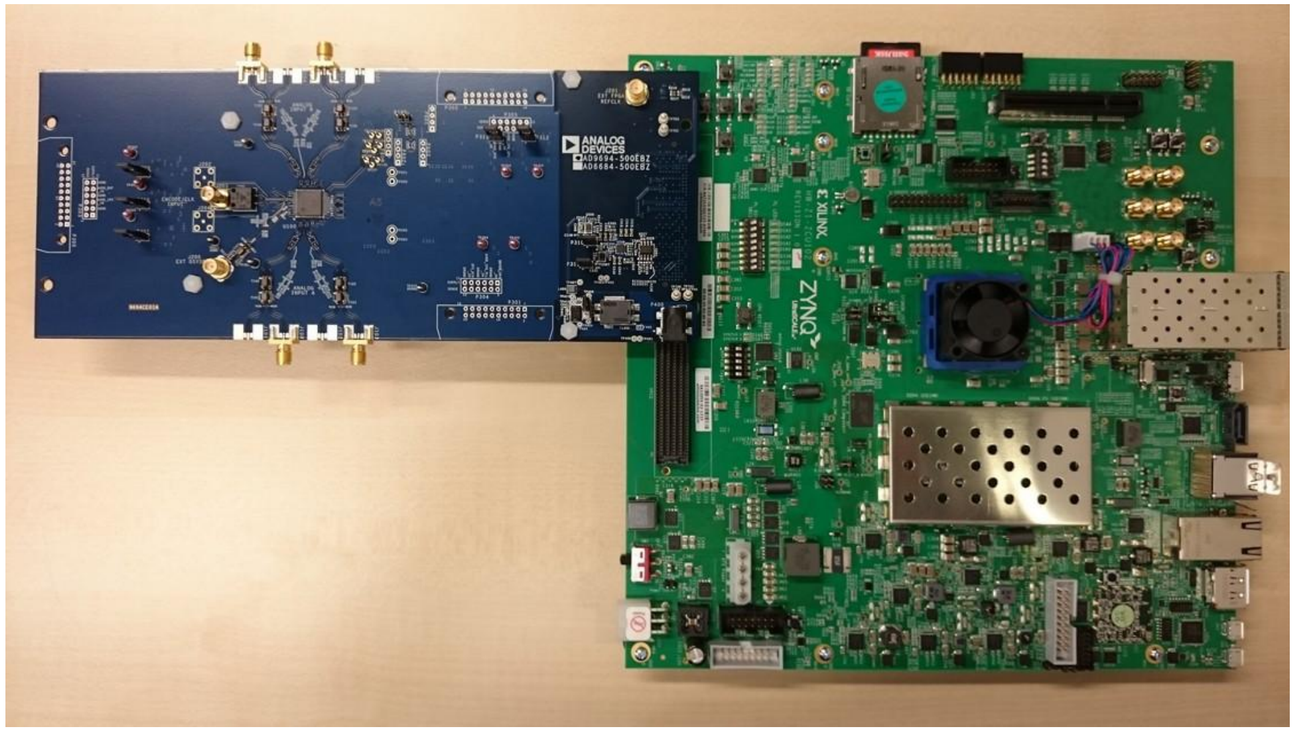
“SMALL” before “GRAND” ???
→ Not really!

Installment in May 2013 in Argentina
100 antennas
6 km2



Merge Analog Devices with Xilinx ref design

Analog Devices
ad9694-500ebz
reference board



Xilinx ZCU102
reference board

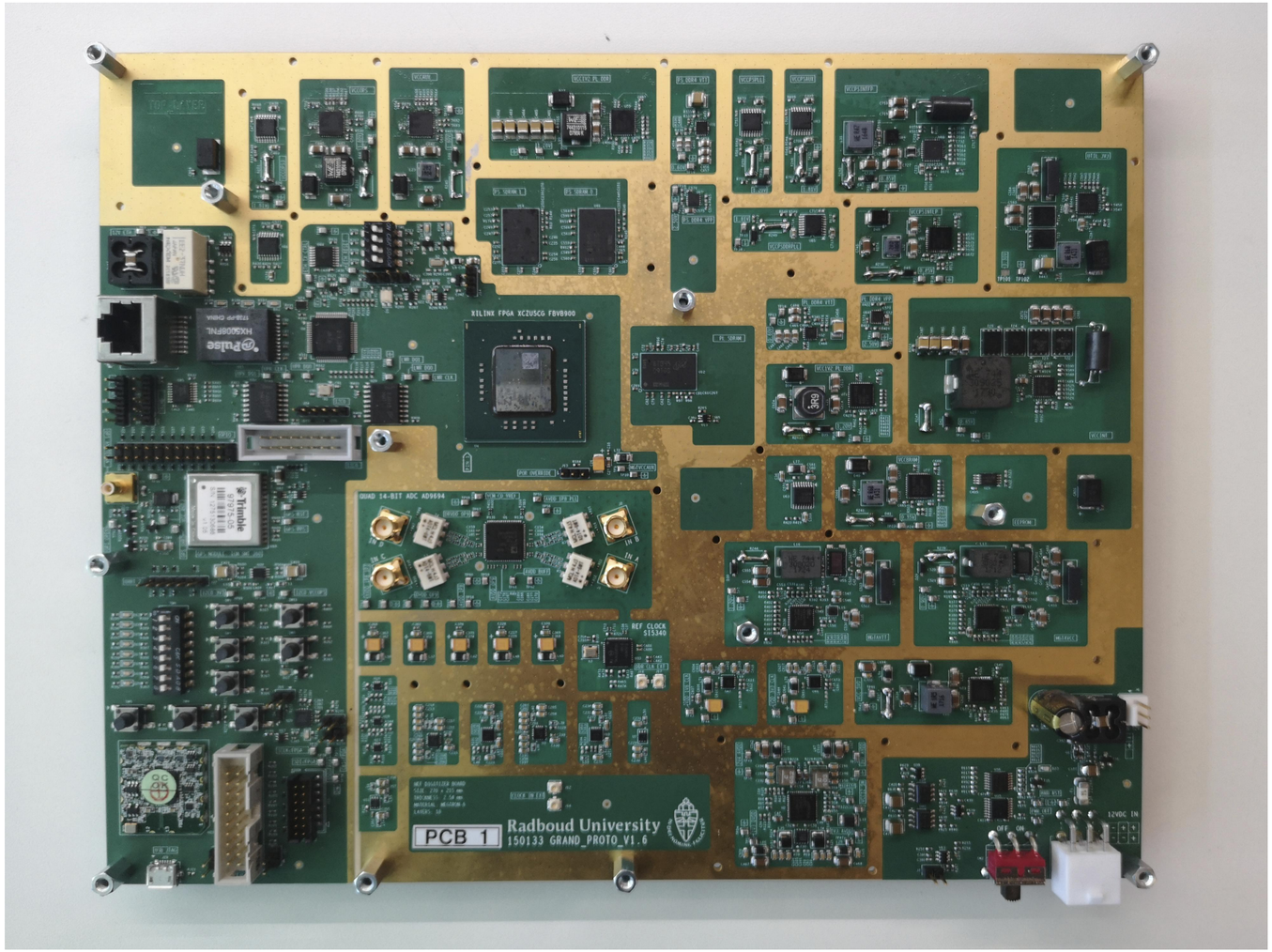
Both companies provide schematics, BoM, board layout

GRAND prototype V1

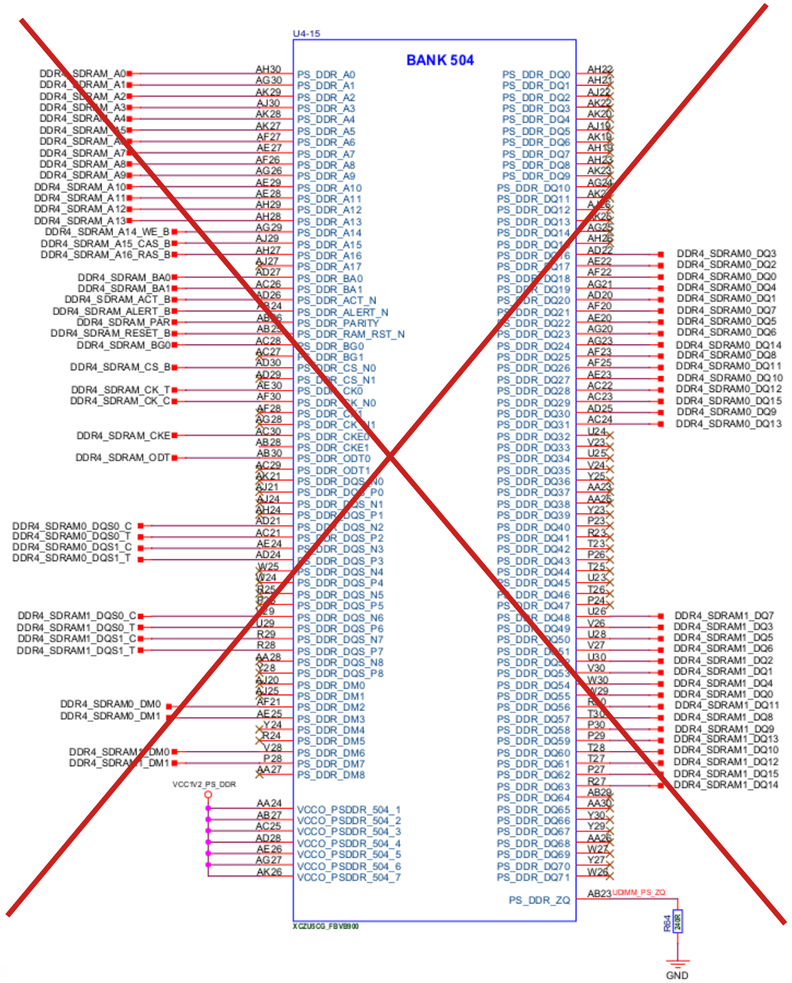
Key features DAQ
Trigger logic and control
FPGA+CPU
ZynqMP: XCZU7CG-1FBVB900E

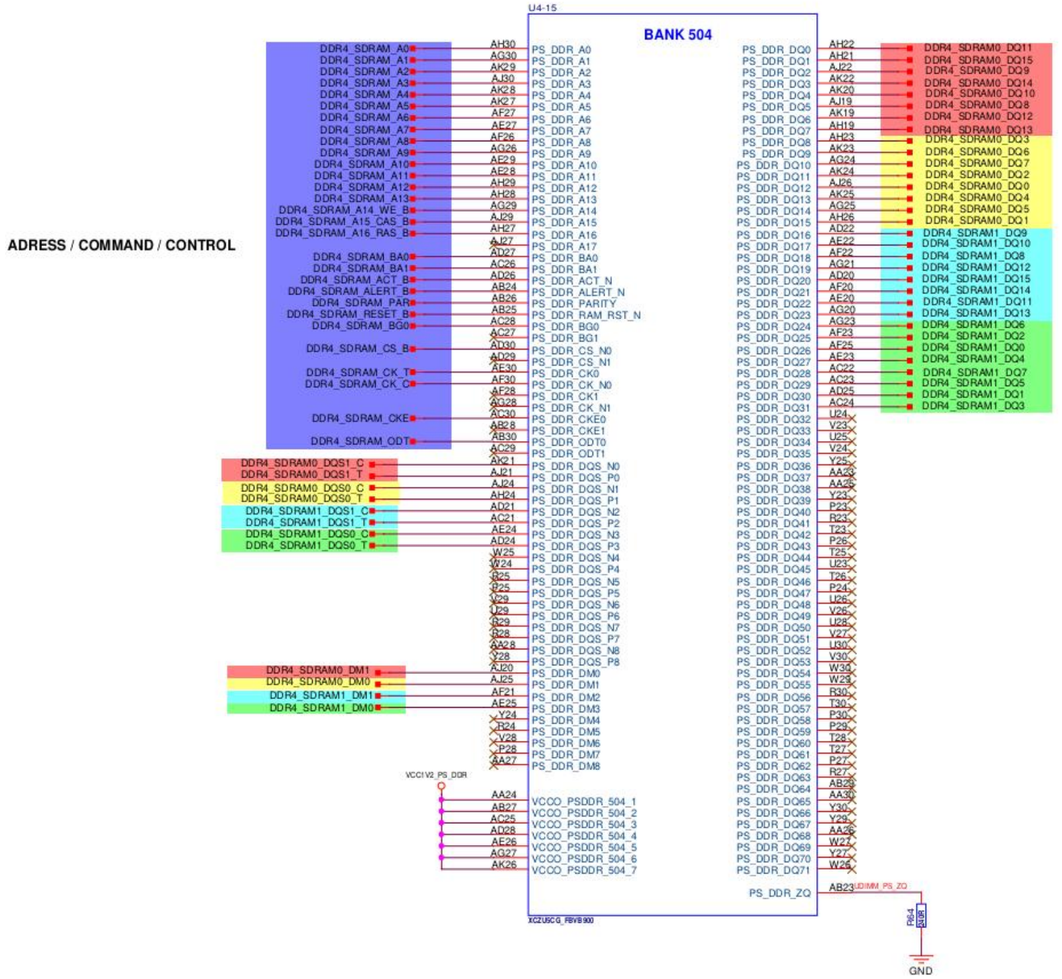
4 channels
14 bit, 500MSPS ADC
30 – 200 MHz
GPS position and timing
Long range WiFi data transfer

Start development towards a more integrated, reliable and cheap DAQ while using less power.

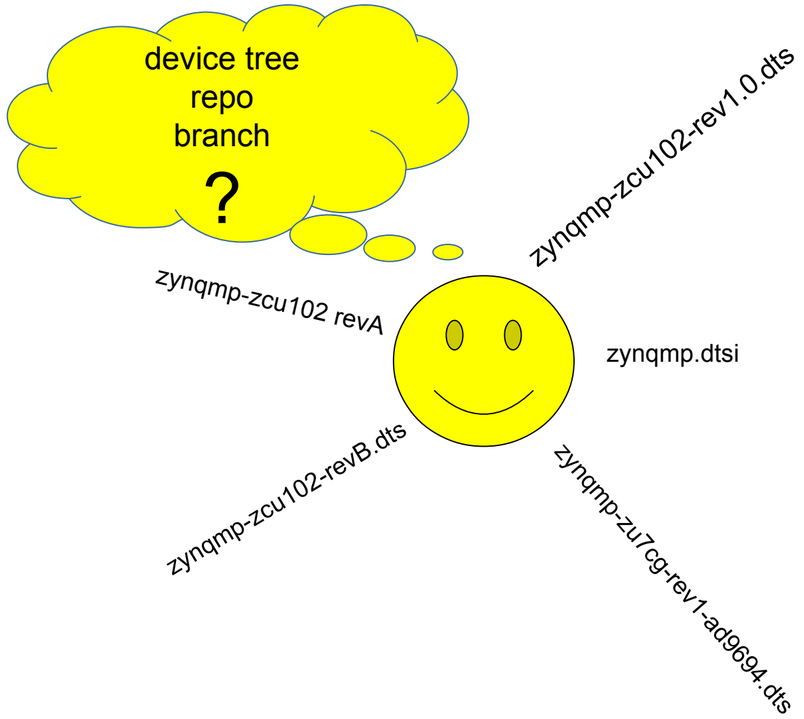


DDR4 memory


U4-15
BANK 504
XCZU5CG_FBVB900
VCCIO_PSDDR_504_1
VCCIO_PSDDR_504_2
VCCIO_PSDDR_504_3
VCCIO_PSDDR_504_4
VCCIO_PSDDR_504_5
VCCIO_PSDDR_504_6
VCCIO_PSDDR_504_7
VCCIO2_PS_DDR
PS_DDR_ZQ
UDIMM_PS_ZQ
GND


ADRESS / COMMAND / CONTROL
U4-15
BANK 504
XCZU5CG_FBVB900
VCCIO2_PS_DDR
PS_DDR_ZQ
UDIMM_PS_ZQ
GND
BYTELANE 0
SDRAM 0
BYTELANE 1
BYTELANE 0
SDRAM 1
BYTELANE 1

Device tree



"Building with Petalinux" from Analog Devices works "out of the box" for standards ADC development boards and a number of FPGA boards. (https://wiki.analog.com/resources/tools-software/linux-build/generic/petalinux)

– The Device Tree Compiler (dtc) is an easy tool to get the details of what is actually built

→ dtc -I dtb images/linux/system.dtb -O dts -o ../devicetree/recompiledDTBs/xxx.dts

– But, where is all this information coming from?

→ user layer from meta-adi-xilinx, meta-adi-core, .../project-spec/meta-user/recipes-bsp/device-tree/files/xxx.dts

– And, if you know where it comes from how to modify this to your own needs?
→ Added custom device tree to the files directory and reference it directly in /meta-adi/meta-adi-xilinx/recipes-bsp/device-tree/device-tree.bbappend

QSPI

Boot from QSPI
– Make sure there is a backup solution available.

– Match the size of the “partitions” to the MTD erase size = 131072 (128K) and set this also in Petalinux

– Uncheck “Use small 4096 B erase sectors” in the kernel config (petalinux-config -c kernel)

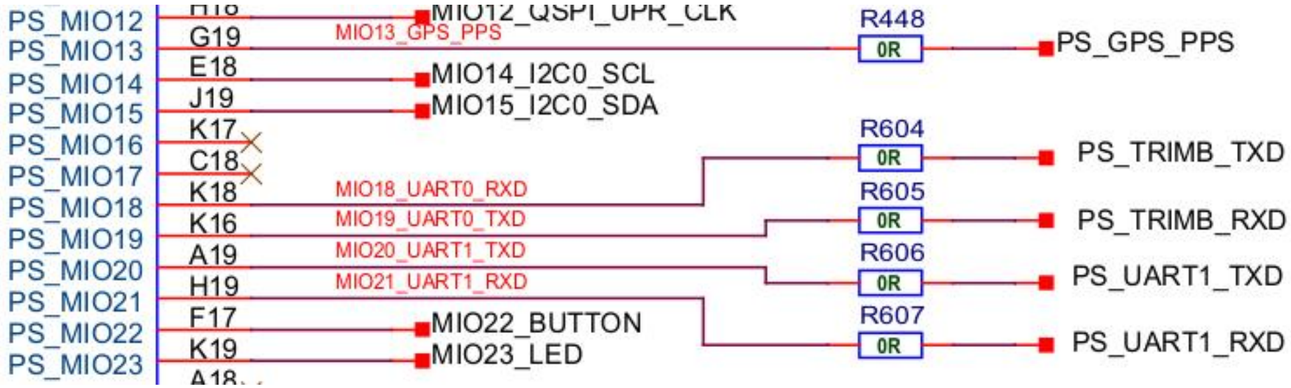
```
&qspi {
    status = "okay";
    is-dual = <1>;
    has-io-mode = <1>;
    /delete-node/ flash@0;
flash@0 {
    compatible = "micron,m25p80", "spi-flash", "n25q512a"; /* dual 512Mb, 1Gb total */
    < – – – snip – – – >

    •partition@boot {
        label = "boot";
        reg = <0x0 0x1e00000>;
    };
    partition@bootenv {
        label = "bootenv";
        reg = <0x1e00000 0x40000>;
    };
    partition@kernel {
        label = "kernel";
        reg = <0x1e40000 0x2400000>;
    };
    partition@jffs2 {
        label = "jffs2";
        reg = <0x4240000 0x2EE0000>;
    };
    partition@spare {
        label = "spare";
        reg = <0x7120000 0x20000>;
};
```

Boot Linux

Set boot arguments in U-boot:
jffs2 boot:
setenv bootargs "console=ttyPS0,115200 earlyprintk
clk_ignore_unused root=mtd:jffs2 rw rootfstype=jffs2"

nfs boot:
setenv bootargs "earlyprintk console=ttyPS0,115200
clk_ignore_unused root=/dev/nfs
nfsroot=192.168.10.1:/srv/nfs,vers=3,nolock,tcp
ip=192.168.10.2:192.168.10.1 rw nfsrootdebug"

– serial interface → never connect the default serial output to the 2nd uart interface on the ZynqMP.



Hardware HDL

Take time to find the best match for the HDL project (PL-firmware), device tree and Linux device drivers (PS-software). The best match depends on the ADC, FPGA, peripherals, clocks and power supplies on the board.

HDL projects:
→ https://github.com/analogdevicesinc/hdl/tree/master/projects

Sometimes the ADC occurs in several ADC hdl projects. It can be beneficial to use a more recent project and accept a mismatch with the used ADC to be able to profit from new (or more flexible) software or firmware.

Start the puzzle here to match the FPGA software version with the HDL release from Analog Devices. Take care, year numbers do not match with FPGA software release! (e.g. release hdl_2019_r1 should be used with Quartus 18.1 or Vivado 2018.3)
→ https://wiki.analog.com/resources/fpga/docs/releases

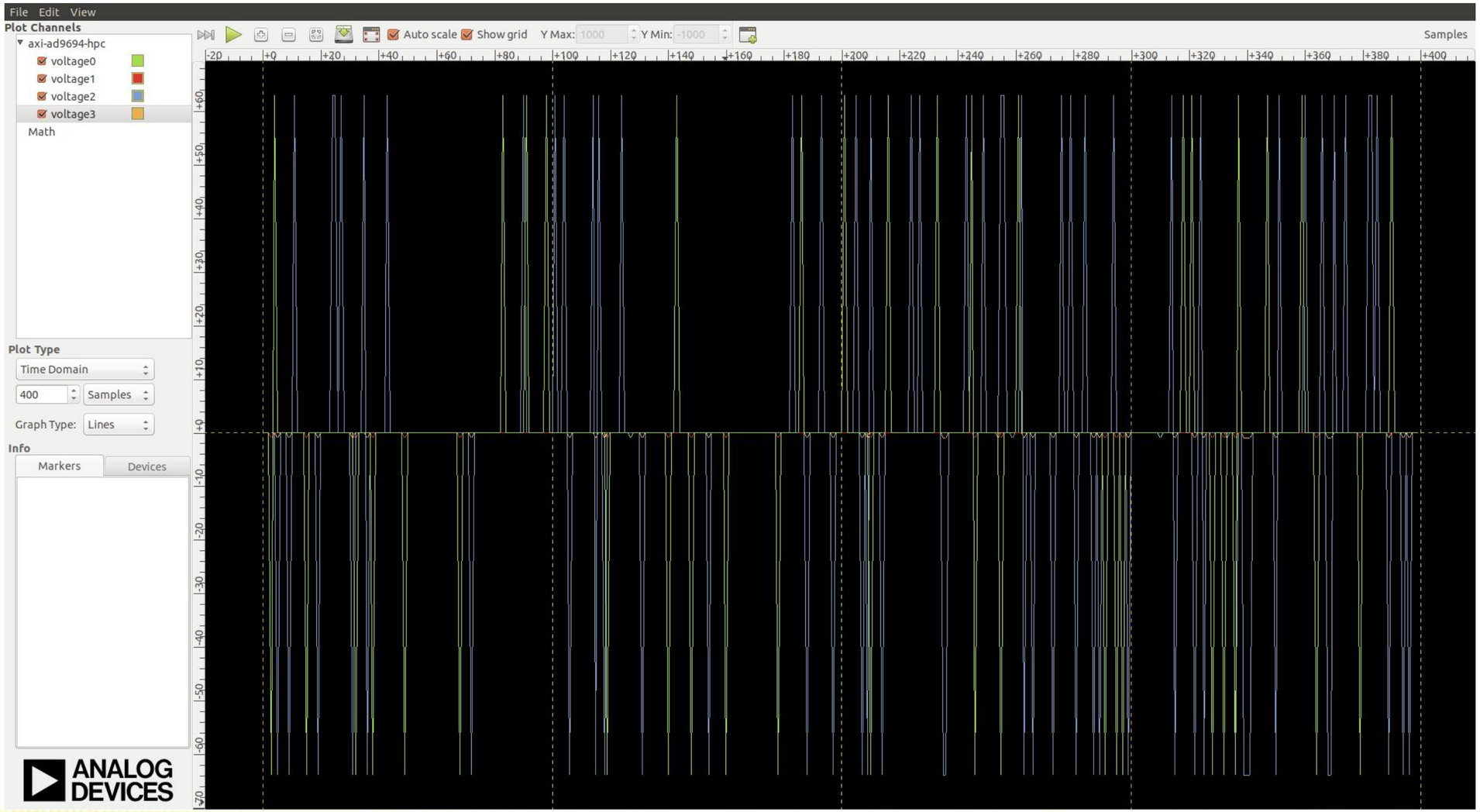
Debug axi busses, hdl, ADC setting and JESD204 lane parameters

Call in help from Analog Devices via EngineerZone forum:
→ https://ez.analog.com/

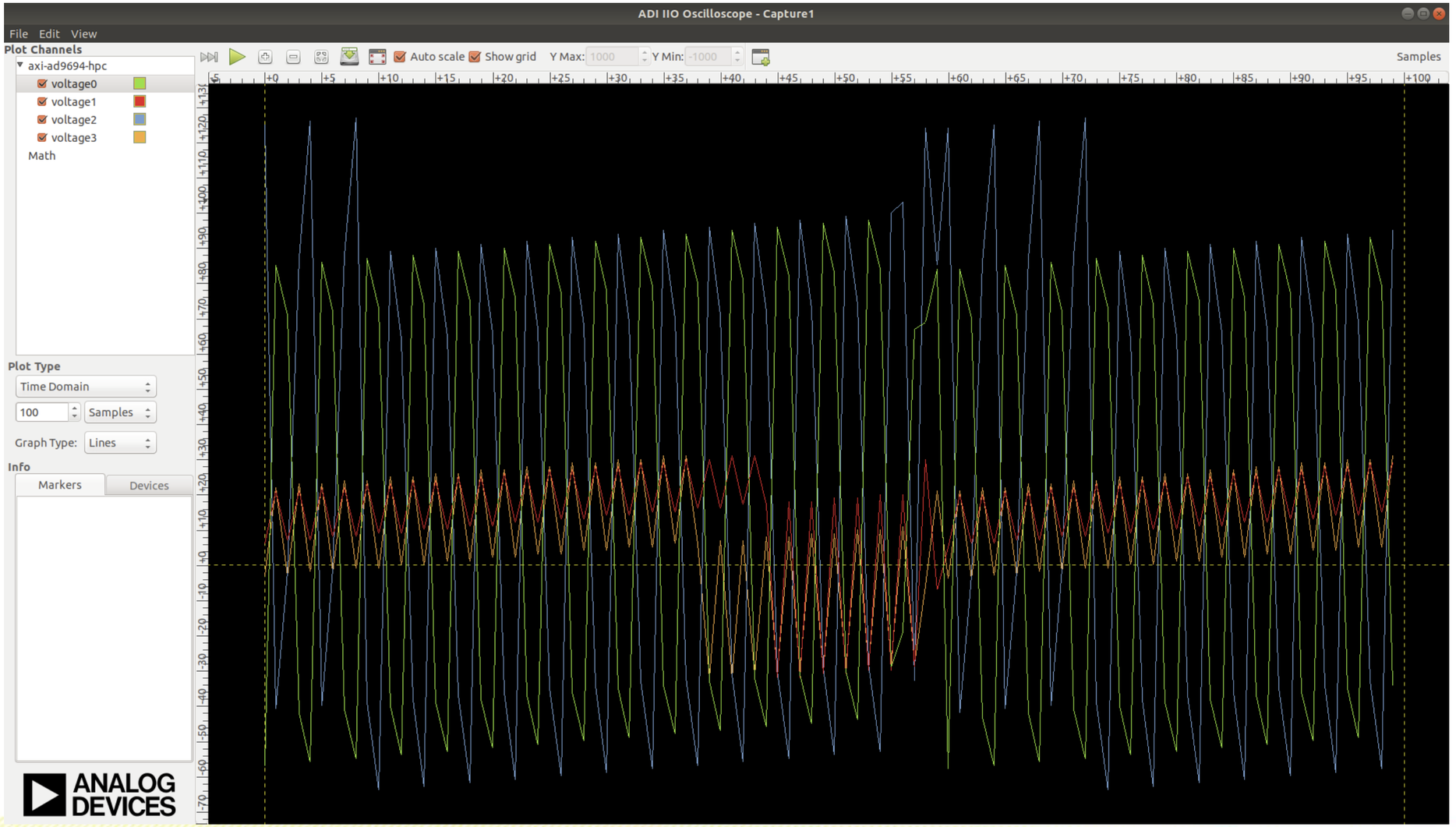
A lot of information can be subtracted from:
grep "" /sys/bus/platform/devices/*.axi-jesd*/status*
grep "" /sys/bus/platform/devices/*.axi-jesd*/lane*

But before the ADC shows up as an IIO device (iio_info):
– take care of clocking (in the device tree)
– make sure the clock can be reconfigured with a “clk_set_rate” from a device driver.
– enable debug messages in device driver add:
  #define DEBUG
  Before the first include and then rebuild your kernel (with the default log level in the kernel config to print debug messages)

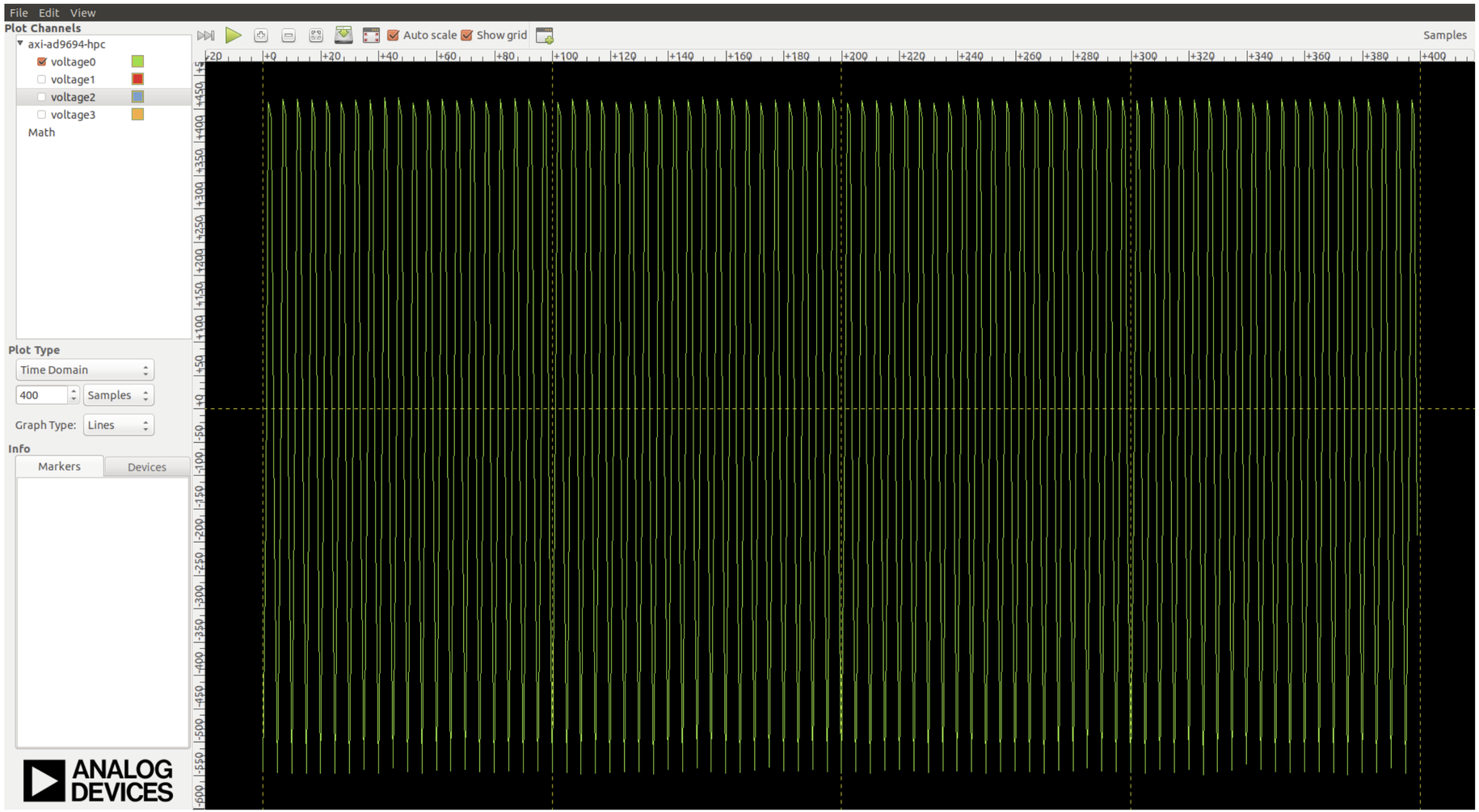
First data


File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 1000
Y Min: -1000
Samples
Plot Type
Time Domain
400
Samples
Graph Type: Lines
Info
Markers
Devices
ANALOG DEVICES

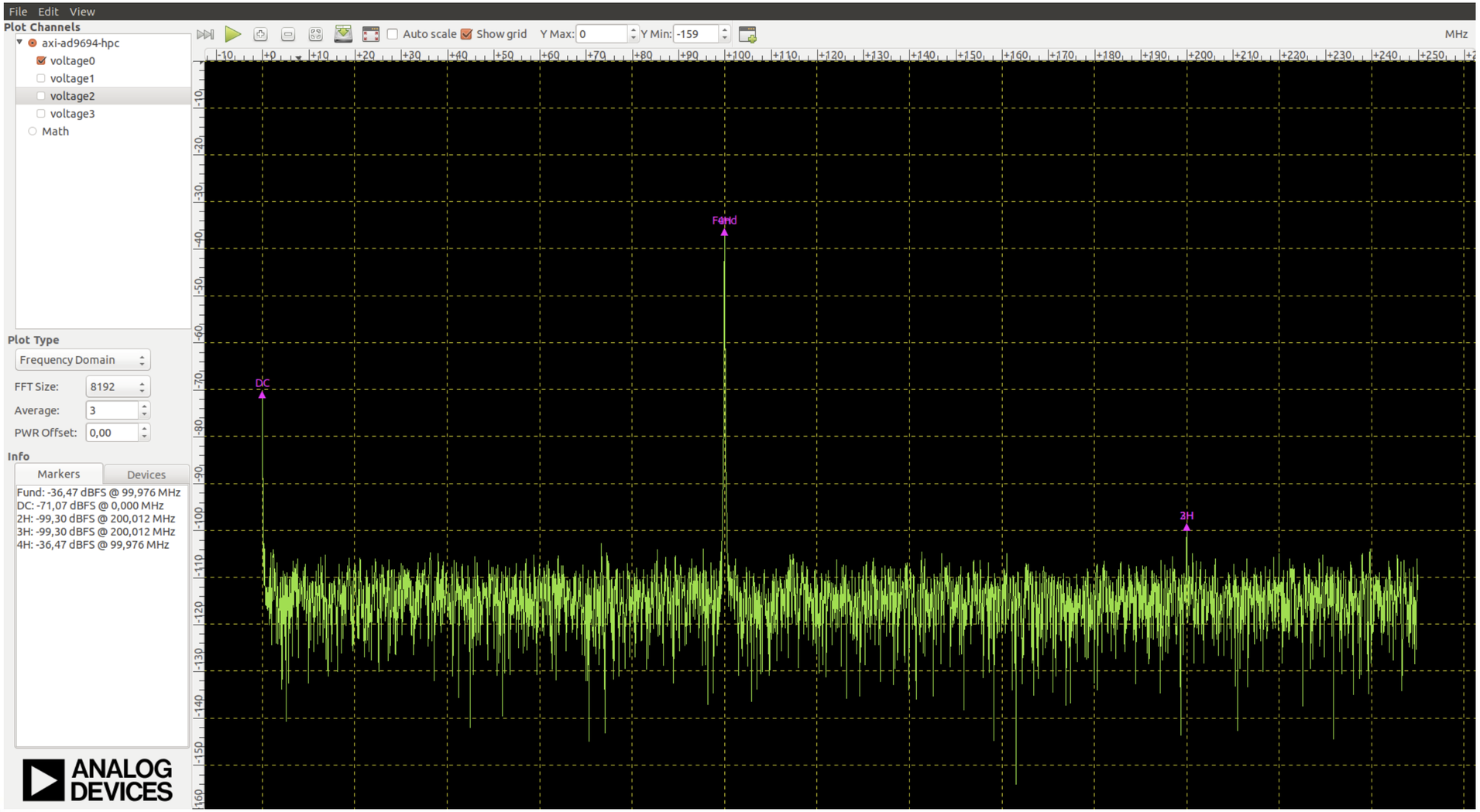
First data


ADI IIO Oscilloscope - Capture1
File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Plot Type
Time Domain
100
Samples
Graph Type:
Lines
Info
Markers
Devices
Auto scale
Show grid
Y Max:
1000
Y Min:
-1000
Samples
ANALOG DEVICES

Results

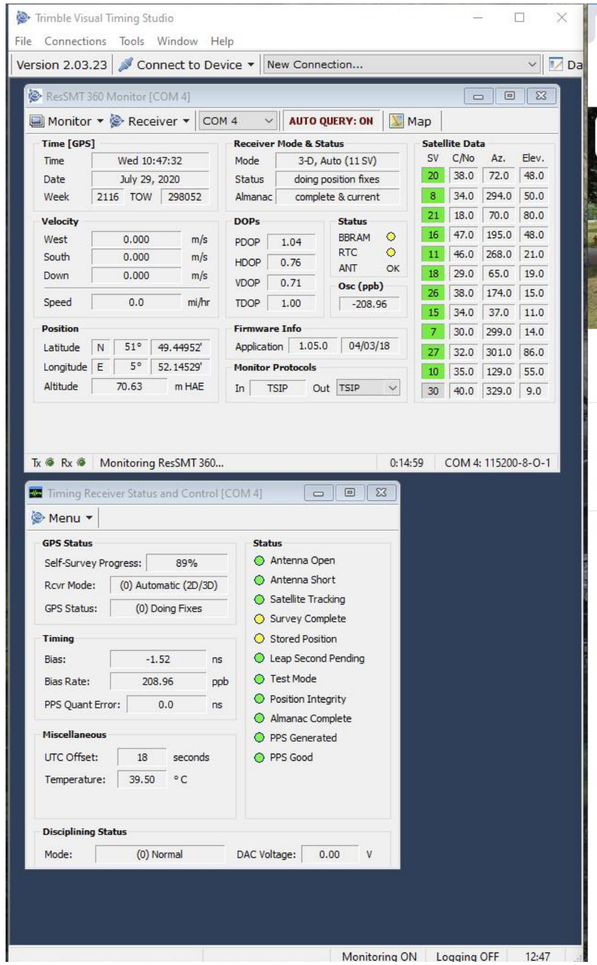

File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Samples
Plot Type
Time Domain
400
Samples
Graph Type:
Lines
Info
Markers
Devices
ANALOG DEVICES

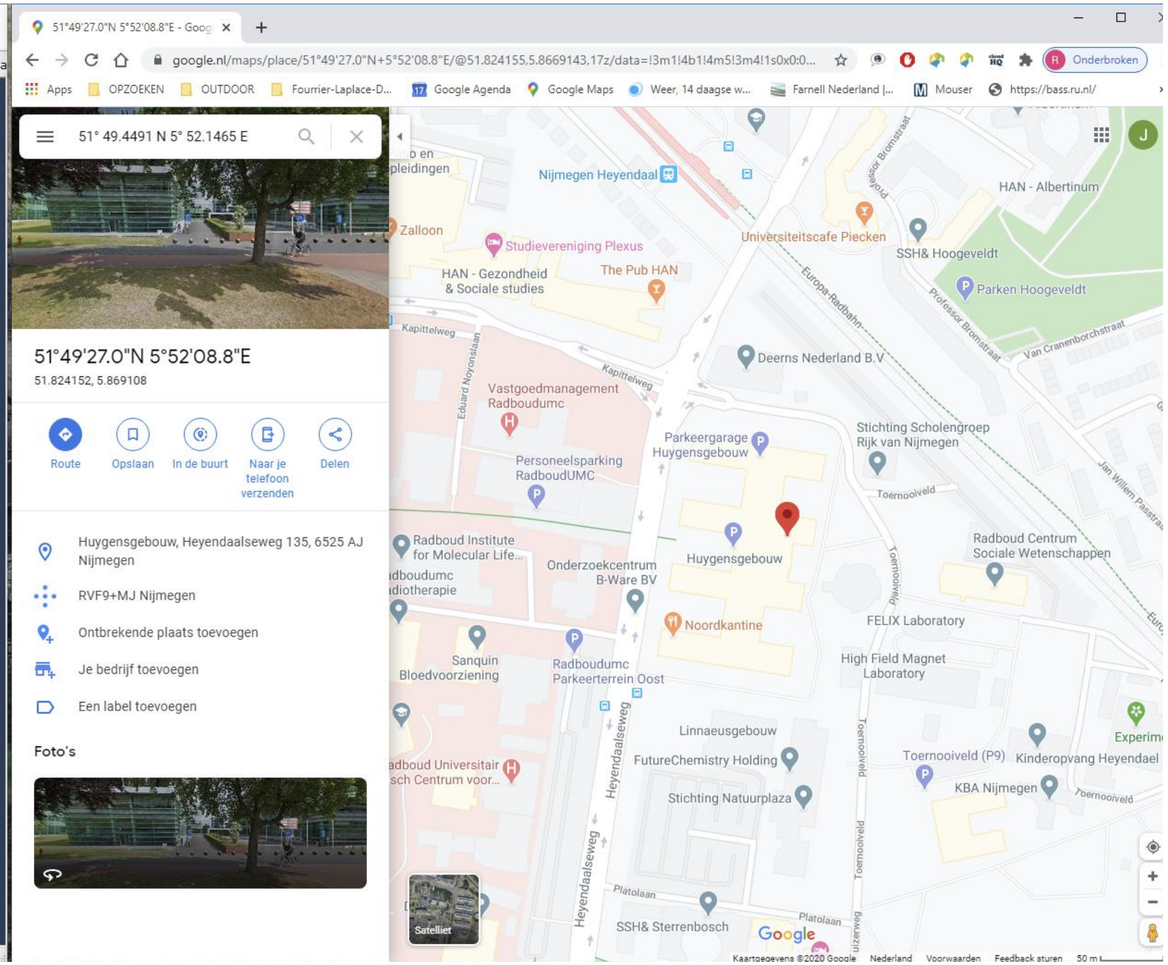
Results


File Edit View
Plot Channels
axi-ad9694-hpc
voltage0
voltage1
voltage2
voltage3
Math
Auto scale
Show grid
Y Max: 0
Y Min: -159
MHz
Plot Type
Frequency Domain
FFT Size: 8192
Average: 3
PWR Offset: 0,00
Info
Markers
Devices
Fund: -36,47 dBFS @ 99,976 MHz
DC: -71,07 dBFS @ 0,000 MHz
2H: -99,30 dBFS @ 200,012 MHz
3H: -99,30 dBFS @ 200,012 MHz
4H: -36,47 dBFS @ 99,976 MHz
ANALOG DEVICES
DC
3H

Results GPS


Amsterdam
Rotterdam
Den Haag
Utrecht
Arnhem
Nijmegen
Antwerpen
Gent
Brussel
Dortmund
Essen
Duisburg
Düsseldorf
Wuppertal
Bonn
Keulen
Satelliet
Google


Trimble Visual Timing Studio
File Connections Tools Window Help
Version 2.03.23
Connect to Device
New Connection...
ResSMT 360 Monitor [COM 4]
Monitor
Receiver
COM 4
AUTO QUERY: ON
Map
Time [GPS]
Time Wed 10:47:32
Date July 29, 2020
Week 2116 TOW 298052
Velocity
West 0.000 m/s
South 0.000 m/s
Down 0.000 m/s
Speed 0.0 mi/hr
Position
Latitude N 51° 49.44952'
Longitude E 5° 52.14529'
Altitude 70.63 m HAE
Receiver Mode & Status
Mode 3-D, Auto (11 SV)
Status doing position fixes
Almanac complete & current
DOPs
PDOP 1.04
HDOP 0.76
VDOP 0.71
TDOP 1.00
Status
BBRAM
RTC
ANT OK
Osc (ppb)
-208.96
Firmware Info
Application 1.05.0 04/03/18
Monitor Protocols
In TSIP Out TSIP
Satellite Data
SV C/No Az. Elev.
20 38.0 72.0 48.0
8 34.0 294.0 50.0
21 18.0 70.0 80.0
16 47.0 195.0 48.0
11 46.0 268.0 21.0
18 29.0 65.0 19.0
26 38.0 174.0 15.0
15 34.0 37.0 11.0
7 30.0 299.0 14.0
27 32.0 301.0 86.0
10 35.0 129.0 55.0
30 40.0 329.0 9.0
Tx Rx Monitoring ResSMT 360...
0:14:59
COM 4: 115200-8-O-1
Timing Receiver Status and Control [COM 4]
Menu
GPS Status
Self-Survey Progress: 89%
Rcvr Mode: (0) Automatic (2D/3D)
GPS Status: (0) Doing Fixes
Timing
Bias: -1.52 ns
Bias Rate: 208.96 ppb
PPS Quant Error: 0.0 ns
Miscellaneous
UTC Offset: 18 seconds
Temperature: 39.50 °C
Disciplining Status
Mode: (0) Normal
DAC Voltage: 0.00 V
Status
Antenna Open
Antenna Short
Satellite Tracking
Survey Complete
Stored Position
Leap Second Pending
Test Mode
Position Integrity
Almanac Complete
PPS Generated
PPS Good
Monitoring ON
Logging OFF
12:47


51°49'27.0"N 5°52'08.8"E - Google Chrome
google.nl/maps/place/51°49'27.0"N+5°52'08.8"E/@51.824155,5.8669143,17z/data=!3m1!4b1!4m5!3m4!1s0x0:0...
Onderbroken
Apps OPZOEKEN OUTDOOR Fourrier-Laplace-D... Google Agenda Google Maps Weer, 14 daagse w... Farnell Nederland |... Mouser https://bass.ru.nl/
51° 49.4491 N 5° 52.1465 E
51°49'27.0"N 5°52'08.8"E
51.824152, 5.869108
Route
Opslaan
In de buurt
Naar je telefoon verzenden
Delen
Huygensgebouw, Heyendaalseweg 135, 6525 AJ Nijmegen
RVF9+MJ Nijmegen
Ontbrekende plaats toevoegen
Je bedrijf toevoegen
Een label toevoegen
Foto's
Nijmegen Heyendaal
Zalloon
Studievereniging Plexus
HAN - Gezondheid & Sociale studies
The Pub HAN
Universiteitscafe Piecken
HAN - Albertinum
SSH& Hoogeveldt
Parken Hoogeveldt
Deerns Nederland B.V
Vastgoedmanagement Radboudumc
Personeelsparking RadboudUMC
Parkeergarage Huygensgebouw
Stichting Scholengroep Rijk van Nijmegen
Radboud Institute for Molecular Life...
Onderzoekcentrum B-Ware BV
Huygensgebouw
Radboud Centrum Sociale Wetenschappen
Noordkantine
FELIX Laboratory
Sanquin Bloedvoorziening
Radboudumc Parkeerterrein Oost
High Field Magnet Laboratory
Linnaeusgebouw
FutureChemistry Holding
Toernooiveld (P9)
Kinderopvang Heyendael
KBA Nijmegen
Stichting Natuurplaza
SSH& Sterrenbosch
Satelliet
Google
Kaartgegevens ©2020 Google
Nederland
Voorwaarden
Feedback sturen
50 m

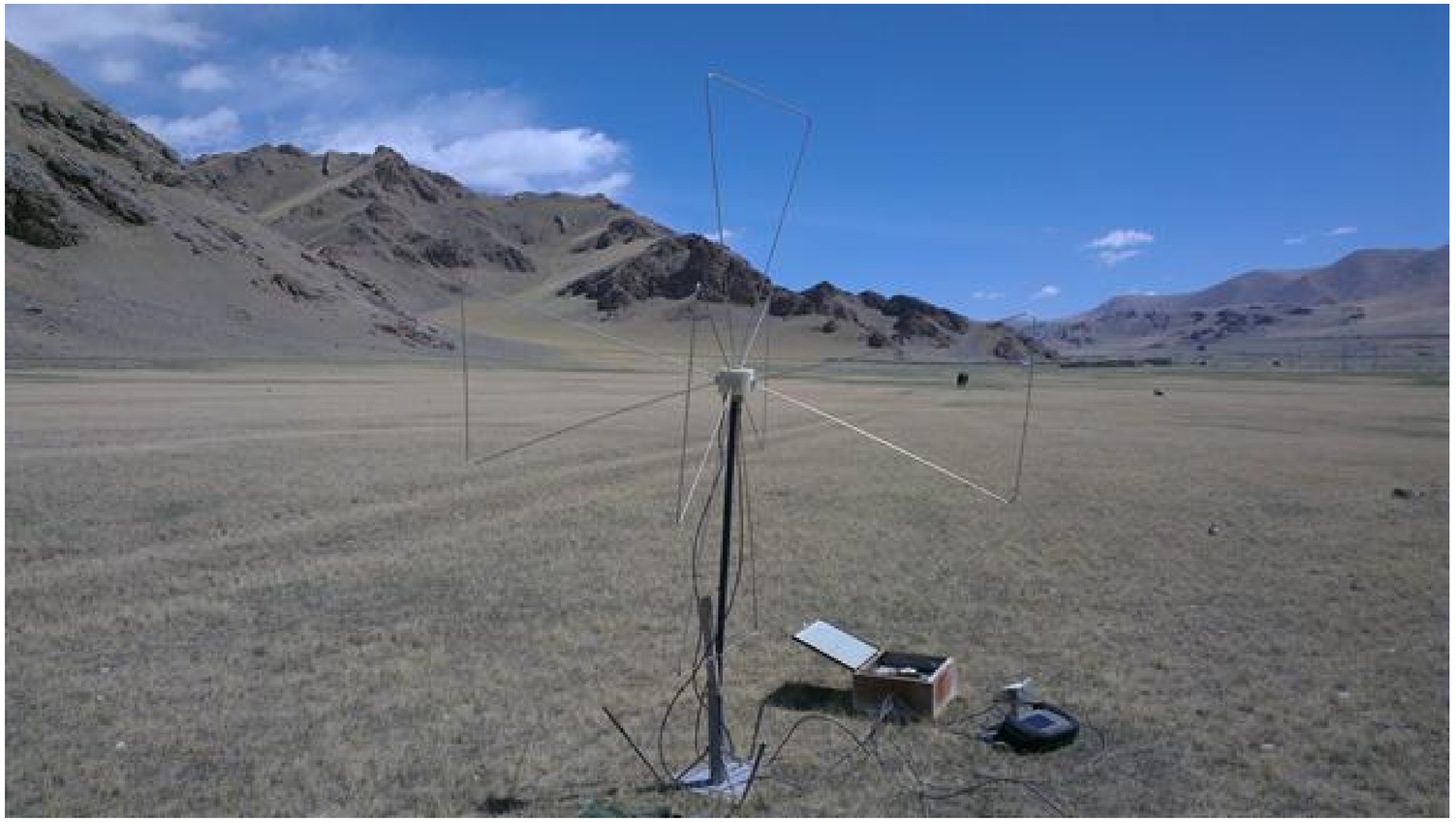
Results

- Testing of first prototype was finished before summer holiday.

- Ready to produce 100 stations using the next iteration of the prototype.

- Next year 100 stations will be installed in remote area in China. Hopefully, 200 more will follow soon after installment

Then there is a lot of work to do to go to 1000, 10.000 and 100.000.



Lessons learned

- It takes a lot of time to debug the boot from QSPI memory. Mainly building and programming the flash.
- Select the Analog Devices HDL project based on available knowledge in you(r team) and on the daq board.
- Learn git, how to make a patch in git and how to apply this patch in Yocto / Petalinux. To be able to add new code you sometimes need a patch…
- Invest time in the development environment especially when booting from QSPI memory. Switch to NFS boot as soon as possible.
- During boot do not reconfigure the clock (chip) that provides the ps_ref_clk. (Thanks Pieter and Ralf :-))
- A clock is not a static signal with a fixed frequency. During boot the device driver of Analog Devices tries several clock settings to be able to set up the JESD204 interface correctly.

- You learn a lot from making your “own” high speed data acquisition board.

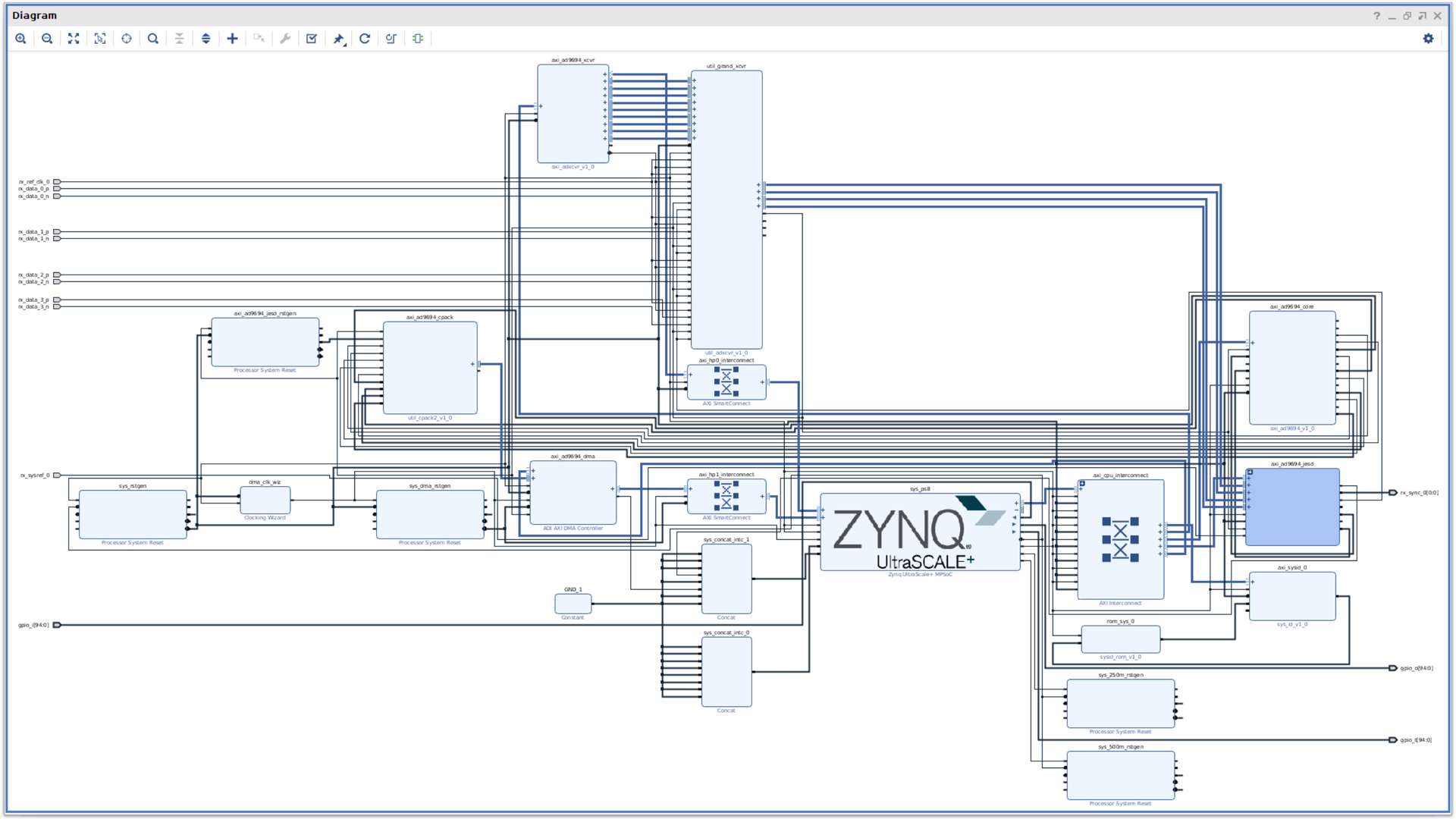
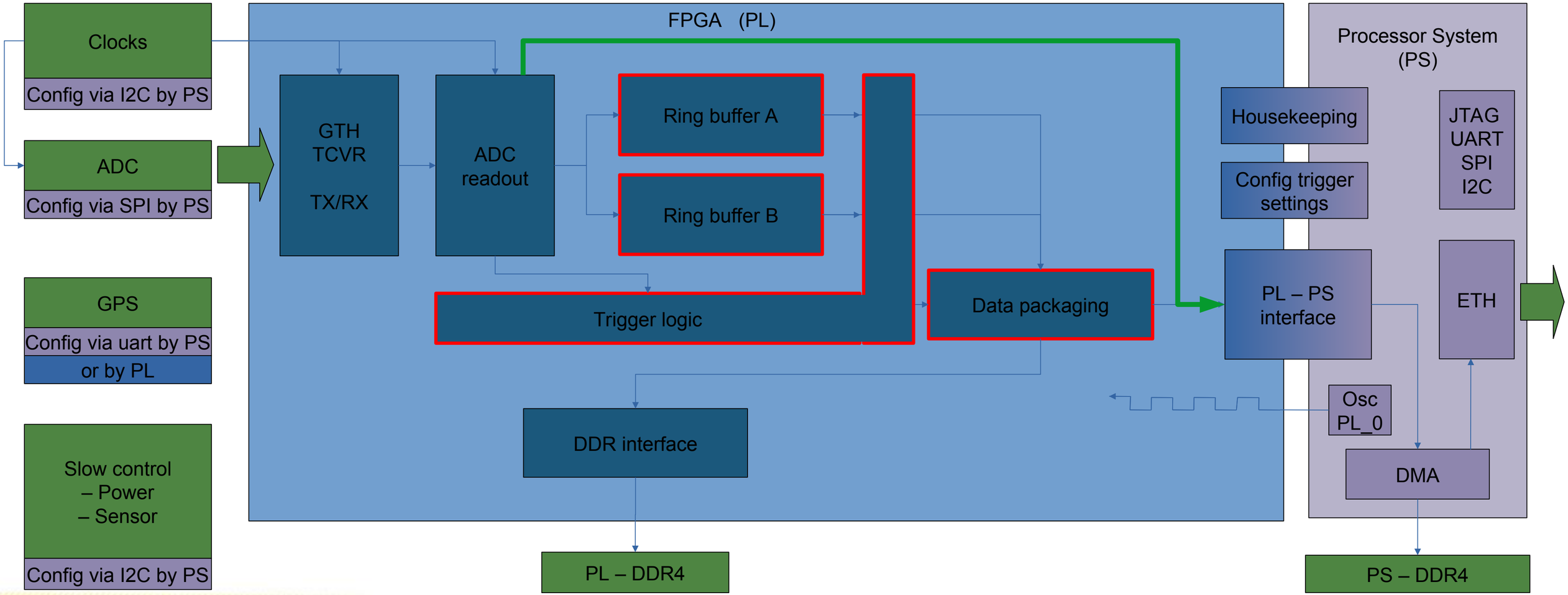
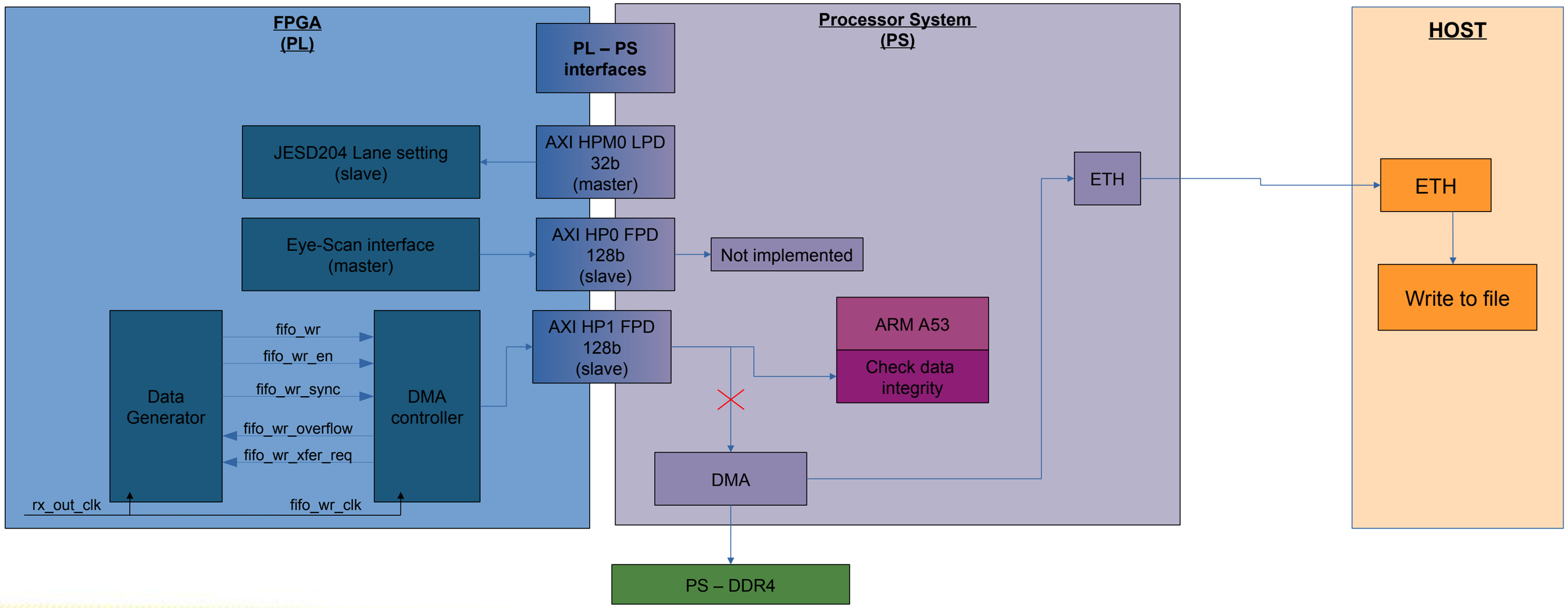


Diagram
axi_ad9694_xcvr
axi_adxcvr_v1_0
util_gtand_xcvr
util_adxcvr_v1_0
rx_ref_clk_0
rx_data_0_p
rx_data_0_n
rx_data_1_p
rx_data_1_n
rx_data_2_p
rx_data_2_n
rx_data_3_p
rx_data_3_n
axi_ad9694_jesd_rstgen
Processor System Reset
axi_ad9694_cpack
util_cpack2_v1_0
axi_hp0_interconnect
AXI SmartConnect
axi_ad9694_core
axi_ad9694_v1_0
axi_ad9694_dma
ADI AXI DMA Controller
axi_hp1_interconnect
AXI SmartConnect
axi_ad9694_jesd
rx_sync_0[0:0]
rx_sysref_0
sys_rstgen
Processor System Reset
dma_clk_wiz
Clocking Wizard
sys_dma_rstgen
Processor System Reset
sys_ps8
ZYNQ
UltraSCALE+
Zynq UltraScale+ MPSoC
axi_cpu_interconnect
AXI Interconnect
axi_sysid_0
sysid_rom_v1_0
rom_sys_0
sys_concat_intc_1
Concat
GND_1
Constant
gpio_i[94:0]
sys_concat_intc_0
Concat
gpio_o[94:0]
sys_250m_rstgen
Processor System Reset
gpio_t[94:0]
sys_500m_rstgen
Processor System Reset

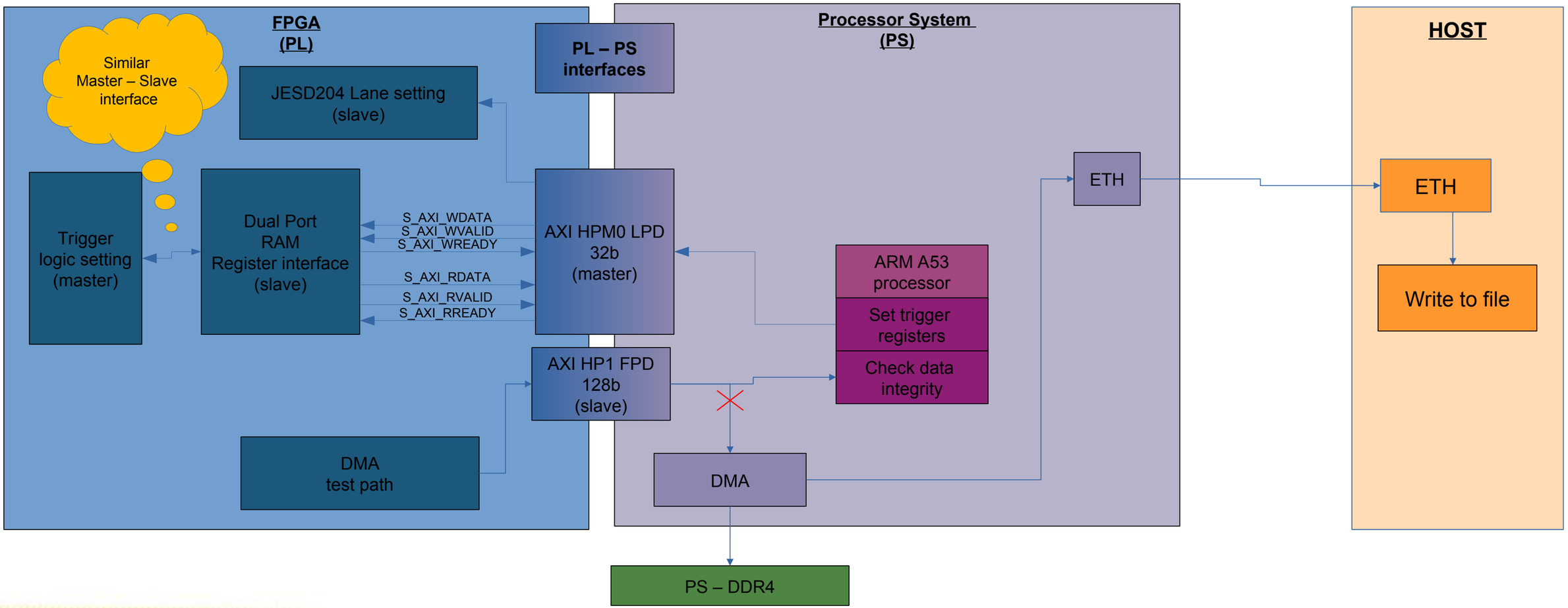
Firmware setup



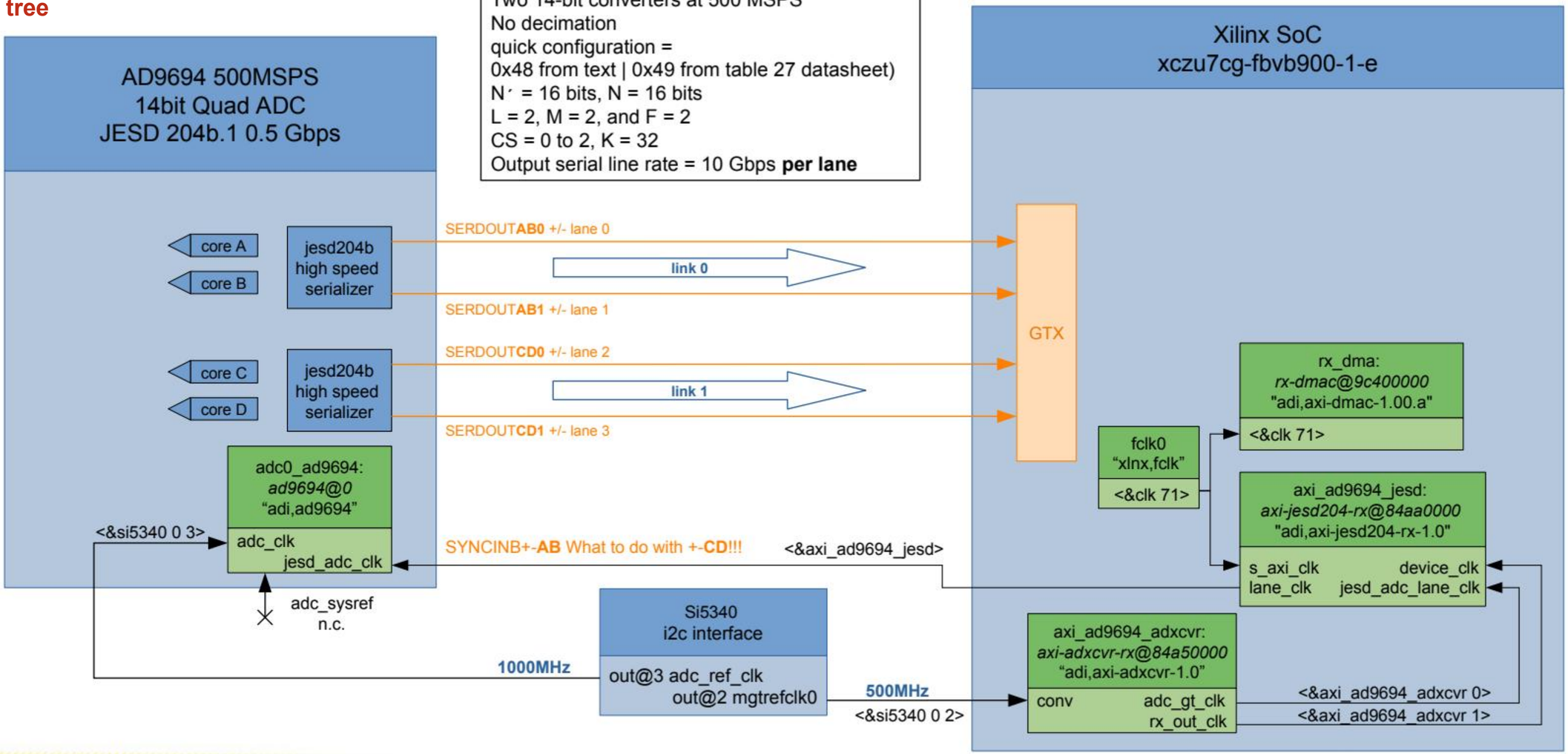
Firmware setup test:
DMA and data througput



Firmware setup test: config trigger logic



Clock config
– Linux device tree



Linux device tree

Per LINK! – full BW mode
Two 14-bit converters at 500 MSPS
No decimation
quick configuration =
0x48 from text | 0x49 from table 27 datasheet)
N´ = 16 bits, N = 16 bits
L = 2, M = 2, and F = 2
CS = 0 to 2, K = 32
Output serial line rate = 10 Gbps **per lane**